

**FOXCONN CONFIDENTIAL**  
**DO NOT DISTRIBUTE**

PAGE	TITLE
01	TOC / SCH INDEX
02	PROJECT INFO
03	BLOCK DIAGRAM
04	CLOCKS DIAGRAM
05	POWER FLOW DIAGRAM
06	POWER GOOD DIAGRAM
07	POWER SEQUENCE DIAGRAM
08	TCM, AssertID, TCM Header
09	CLOCK GEN - CK505 32PIN
10	Intel XDP/DMI Debug header
11	MCP- CLK, CTRL, MISC, DEBUG
12	MCP- DDR3 CHANNEL A
13	MCP- PCIE, DMI, FDI
14	MCP VCCP CONNECTIONS
15	MCP- VCC_DDR, 1_1VAXG, GND
16	PCH DEBUG PORT
17	DDR3 CH-A DIMM1
18	DDR3 CH-A DIMM2
19	DDR3 CH-B DIMM1
20	DDR3 CH-B DIMM2
21	PCH- DMI, PCIE, USB
22	PCH - PCI & NVRAM
23	PCH - SATA, MLINK, GPIO
24	PCH - MISC, GPIO, SMBUS
25	PCH - DP, IPLINK, NVRAM
26	PCH - POWER & GND
27	PCH-PLL FILTER & DCPING
28	Front USB Port
29	AUDIO CODEC
30	AUDIO CONNECTOR
31	SATA
32	RJ45_USB 2.0 CONNECTORS
33	Blank
34	PCI 2.3 - PCI Slot 1
35	PCI 2.3 - PCI Slot 2
36	PCIEx1
37	PCIEx16 Slot
38	PCIEx16
39	SuperIO NCT6681F
40	None

PAGE	TITLE
41	FRONT PANEL & DSW
42	SPI EEPROM
43	Serial Port, Thermal Header
44	VGA
45	DISPLAY PORT CONNECTOR
46	POWER INPUT & EMI CAP
47	LED
48	FAN HEADERS
49	Lewisville ( 82578LM )
50	+5V_DUAL
51	+3P3V_AUX
52	1P8VSFR
53	1P05_ME/ 1P05V_PCH
54	VCC_DDR/ VTT_DDR
55	VCORE
56	X-VCORE PHASE 1 & 2
57	X-VCORE PHASE 3 & 4
58	+1P1V_AXG
59	VCCP_VTT
60	VCCSA
61	EUP&+LPS
62	PCH GPIO Information
63	SIO/Others GPIO Information
64	Strapping Information
65	Changelist

# Lenovo IS6XM - uATX

## Project Information

Phase: SVT X7 2011/03/18

BOM: SVT 0.4

SVID: 17AA

## BIOS Licence Label

LBL1

BIOS\_LICENCE

Note:

AMI uEFI

Modify Note:  
- PCB Information  
- PCB Stack-up information

## PCB Fab Note

PCB1

Printed Circuit Board

PCB SugarBay-uATX REV:1.0

CRITICAL

4-Layer PCB, Color With Green(347C,348C,349C) Soldermask, White Silkscreen, 243.84mmX243.84mm, Rev:1.0, ROHS 010144A05-575-G

4 LAYER		1080
Description	COPPER (Oz)	Thickness (MILS)
L1-Top Signal Layer	.5 (Before Plating)	1.9(+0.8/-0.8)
Prepreg		2.7(+0.8/-0.4)
L2-Inner1 Layer	1	1.2(+/-10%)
CORE	Fab Vender will adjust Core thickness to achieve overall board	
L3-Inner 2 Layer	1	1.2(+/-10%)
Prepreg		2.7(+0.8/-0.4)
L4-Bottom Signal Layer	.5 (Before Plating)	1.9(+0.8/-0.8)
TOTAL		1.6mm+/-0.1

Phase: SVT Ver:X7 2011/03/18


Project		Tech Name	SVID	SSID	BOM
Manchester	LI	IS6XM	17AA	3070	MANCHESTER-ATX-LI_SOVP_0.6_BOM.xls
	LC				MANCHESTER-ATX-LC_SOVP_0.5_BOM.xls
Ventoux	LI			1025	VENTOUX-ATX-LI_SVT_0.5_BOM.xls
Thames	LI				THAMES-ATX-LI_SVT_0.4_BOM.xls
	LC				THAMES-ATX-LC_SVT_0.3_BOM.xls
Merton	LI			3077	MERTON-ATX-LI_SVT_0.5_BOM.xls
	LC				MERTON-ATX-LC_SVT_0.4_BOM.xls
Edge91	LI			3081	EDGE91-ATX-LI_SDV_0.2_BOM.xls
Changzhou	LC			3071	CHANGZHOU-LC_SVT_0.4_BOM.xls

## BOM DISTRIBUTION RULE

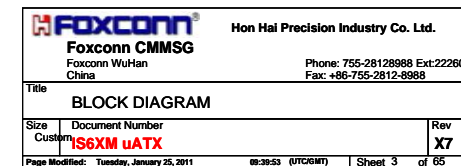
Manchester-LI,Manchester-LC,Ventoux-LI,Thames\_LI,Thames\_LC,Merton-LI,Merton-LC,Edge91-LI,Changzhou-LC

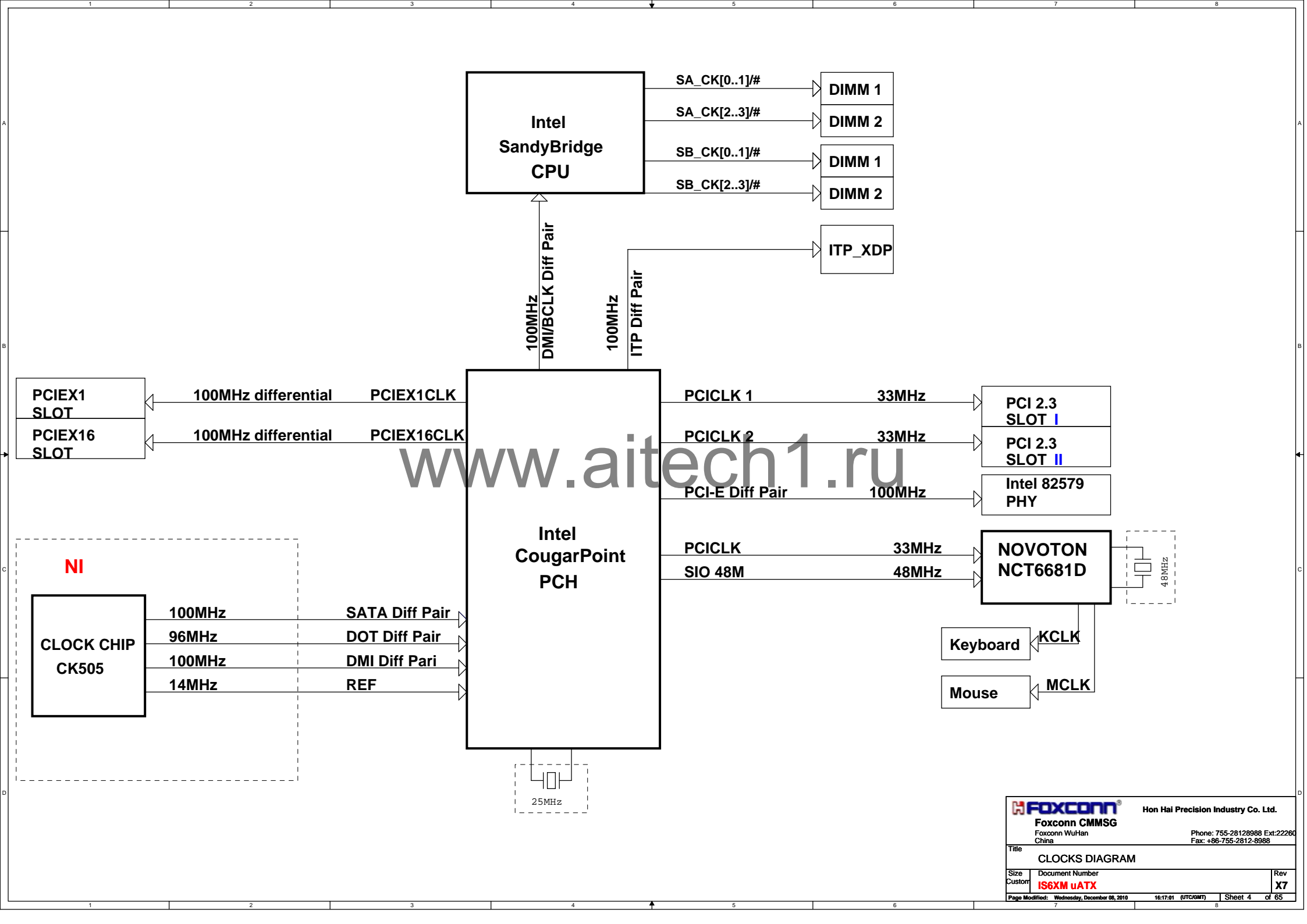
1 2 3 4 5 6 7 8 9

(BOM,BOM,BOM,BOM,BOM,BOM,BOM,BOM,BOM)

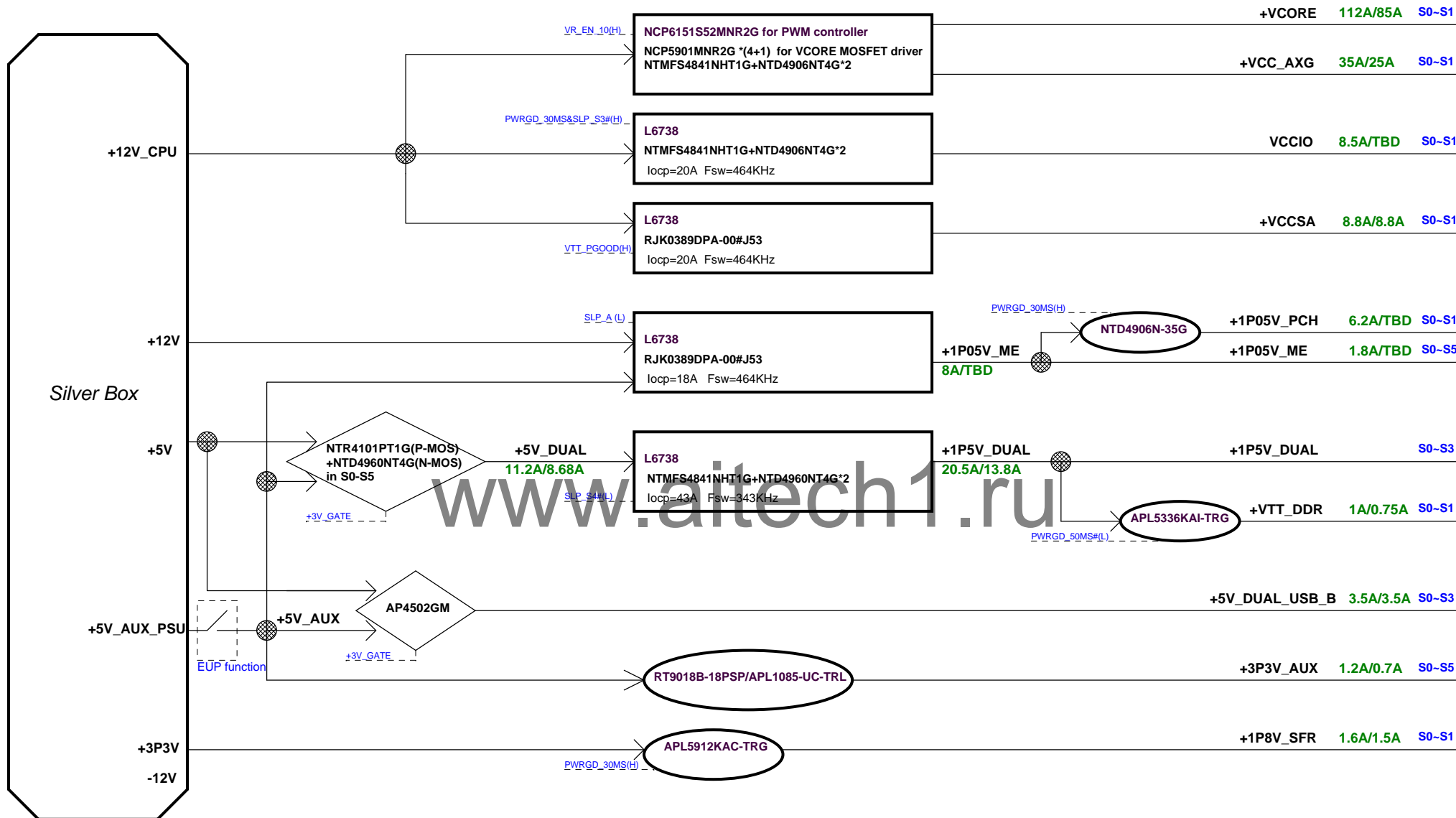
 <b>Foxconn CMMSG</b> Foxconn Wuhan China		Hon Hai Precision Industry Co. Ltd.  Phone: 755-28128988 Ext:22260 Fax: +86-755-2812-8988	
Title			
Project Information			
Size	Document Number		Rev
Custom	IS6XM uATX		X7
Page Modified: Wednesday, March 23, 2011 09:39:58 (UTC+08:00) Sheet 2 of 65			

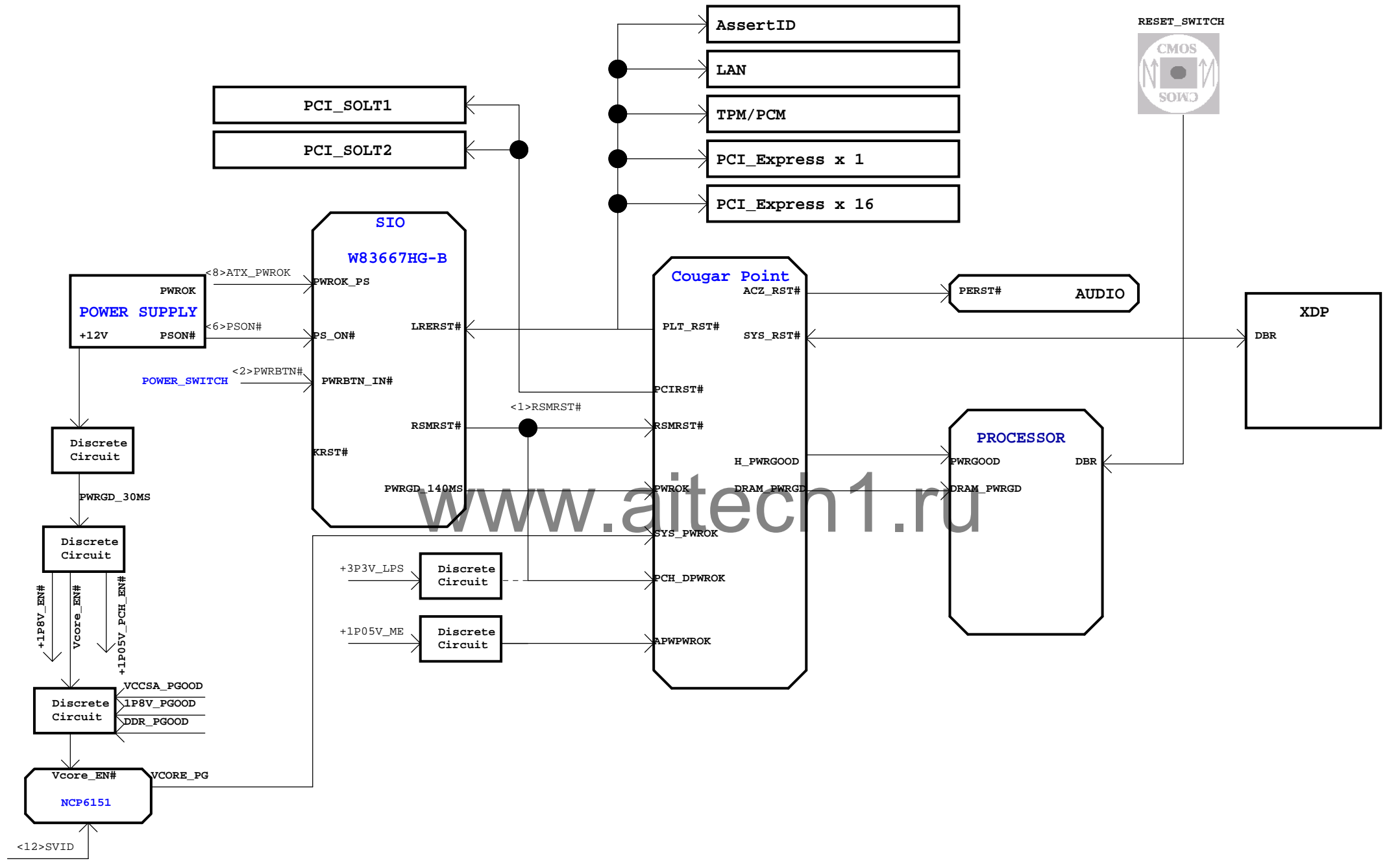
## IS6XM uATX



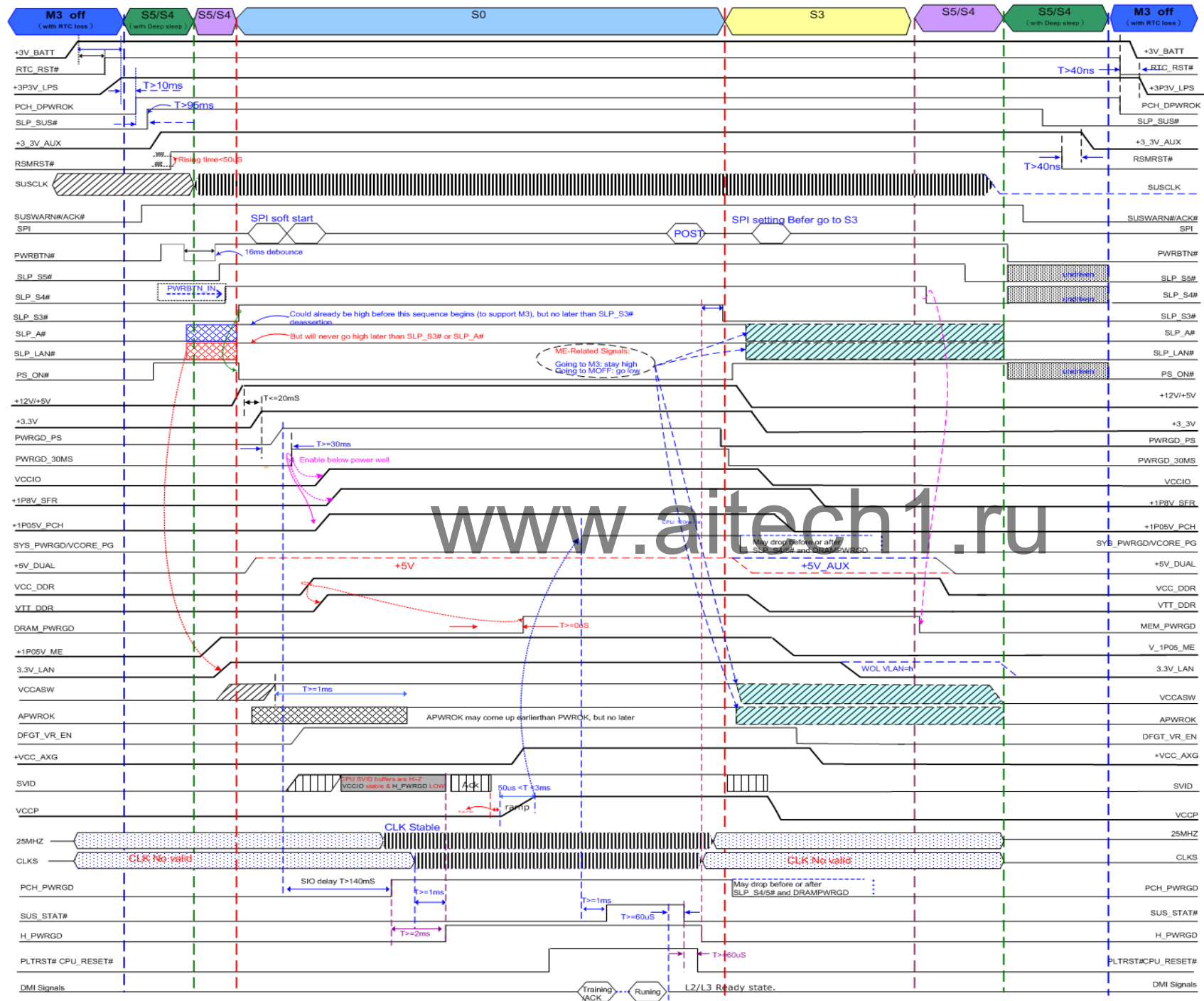








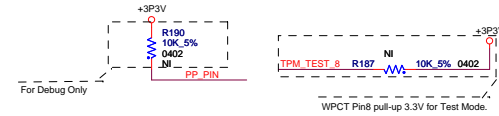
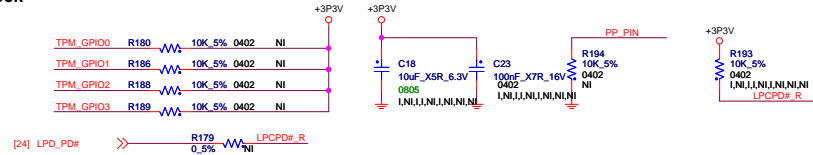
# MANCHESTER POWER SEQUENCE DIAGRAM



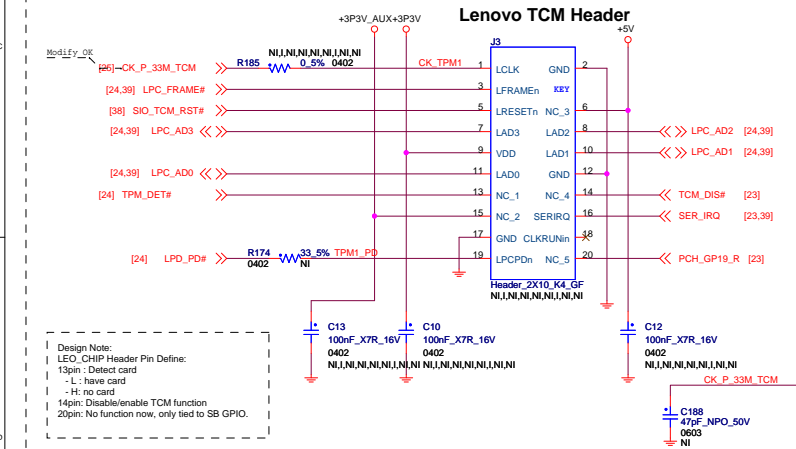
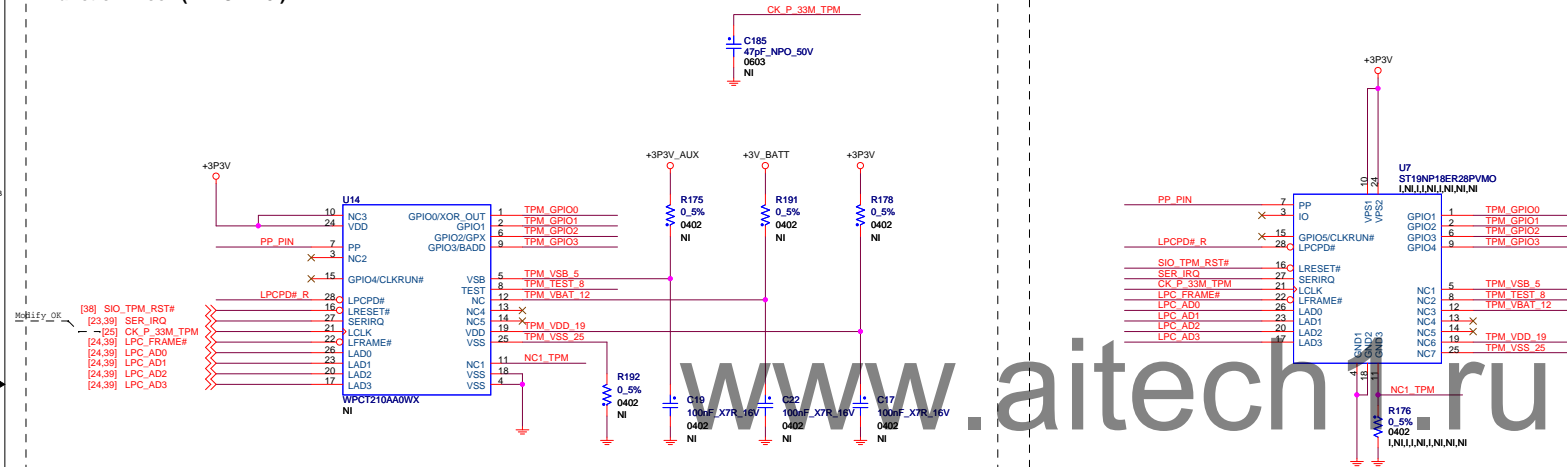
www.aitech1.ru

```
CustomerSpec
Trust Platform Module Spec:
- ST 19NP18
- Winbond WPCT210 (co-lay)
Header:
- TCM Header
CaseOpen
- 1 (Original header and also reserve common 2.54mm header)
```

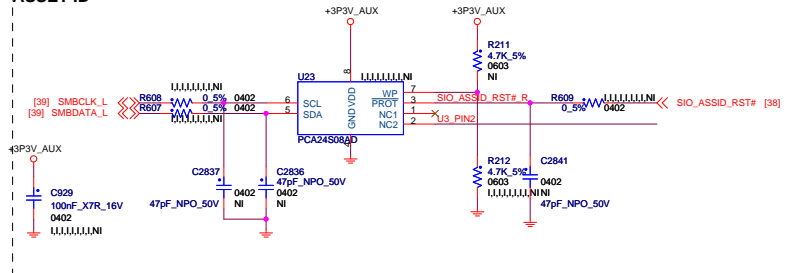
### Common Block



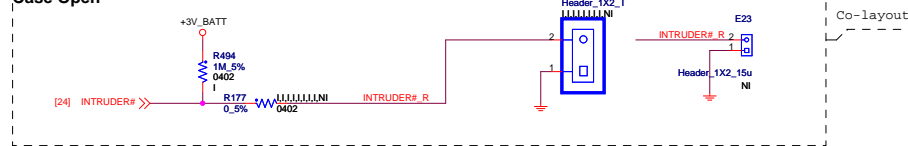
### Function Block ( WPCT210 )




## ASSET ID



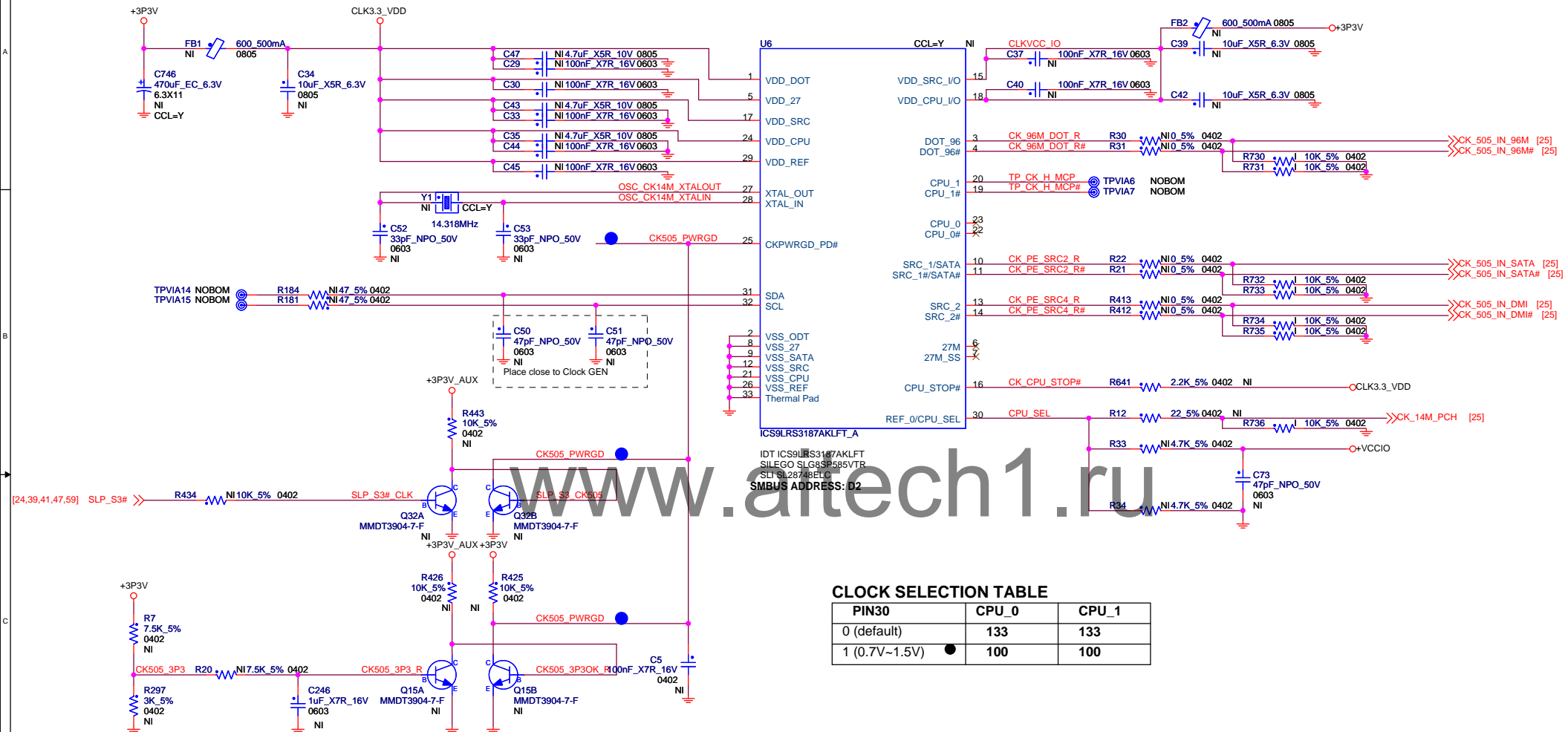
## Case Open



		Hon Hai Precision Industry Co., Ltd.	
<b>Foxconn CMMSG</b> Foxconn Wuhan China		Phone: 755-28128988 Ext.22260 Fax: +86-755-2812-8988	
<b>Title</b> TCM, AssrtID, TCM Header			
<b>Size</b> Custom	Document Number <b>IS6XM uATX</b>		Rev <b>X7</b>
Page Modified: Friday, March 13, 2015		11:30:28 (UTC+08)	Sheet 8 of 65

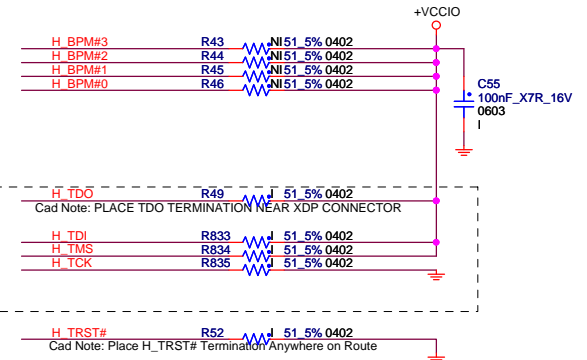
PDG v0.8 page 176: Clock input buffers on PCH that are not driven from CK505 should be terminated properly using one (for REF14 input) or two (for differential inputs) separate 10-kohm pulldown resistors. This is for reliability concerns during platform power-on.

U6	
1	VDD_DOT
5	VDD_27
17	VDD_SRC
24	VDD_CPU
29	VDD_REF
27	XTAL_OUT
28	XTAL_IN
25	CKPWRGD_PD#
31	SDA
32	SCL
2	VSS_ODT
8	VSS_27
9	VSS_SATA
19	VSS_SRC
17	VSS_CPU
26	VSS_REF
33	Thermal Pad



PIN30	CPU_0	CPU_1
0 (default)	133	133
1 (0.7V~1.5V) ●	100	100

**If use XDP Debugging Connector Install "PROTO" Parts and Non-install "MP" Parts(Page25 have "PROTO" Parts)**




Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	GND	GND	NA		2	GND	GND	NA	
3	OBSPFN_A0	PREQ#	I/O	processor 4	4	OBSPFN_C0	CFG[16]	I/O	Processor
5	OBSPFN_A1	PRDY#	I/O	processor 6	5	OBSPFN_C1	CFG[17]	I/O	Processor
7	GND	GND	NA		8	GND	GND	NA	
9	OBSDATA_A0	BPM# [0]	I/O	processor 10	9	OBSDATA_C0	CFG[0]	I/O	Processor
11	OBSDATA_A1	BPM# [1]	I/O	processor 12	11	OBSDATA_C1	CFG[1]	I/O	Processor
13	GND	GND	NA		14	GND	GND	NA	
15	OBSDATA_A2	BPM# [2]	I/O	processor 16	15	OBSDATA_C2	CFG[2]	I/O	Processor
17	OBSDATA_A3	BPM# [3]	I/O	processor 18	17	OBSDATA_C3	CFG[3]	I/O	Processor
19	GND	GND	NA		20	GND	GND	NA	
21	OBSPFN_B0	CFG[10]	I/O	Processor 22	21	OBSPFN_D0	CFG[8]	I/O	Processor
23	OBSPFN_B1	CFG[11]	I/O	Processor 24	23	OBSPFN_D1	CFG[9]	I/O	Processor
25	GND	GND	NA		26	GND	GND	NA	
27	OBSDATA_B0	BPM# [4] / CFG[12]	I/O	processor 28	27	OBSDATA_D0	CFG[4]	I/O	Processor
29	OBSDATA_B1	BPM# [5] / CFG[13]	I/O	processor 30	29	OBSDATA_D1	CFG[5]	I/O	Processor
31	GND	GND	NA		32	GND	GND	NA	
33	OBSDATA_B2	BPM# [6] / CFG[14]	I/O	processor 34	33	OBSDATA_D2	CFG[6]	I/O	Processor
35	OBSDATA_B3	BPM# [7] / CFG[15]	I/O	processor 36	35	OBSDATA_D3	CFG[7]	I/O	Processor
37	GND	GND	NA		38	GND	GND	NA	
39	HOOK0	PWRGOOD	I	system 40	39	ITPCLK/HOOK4	BCLK_ITP	I	processor
41	HOOK1 <sup>†</sup>	BP_PWRGD_RST#	O	system 42	41	ITPCLK#/HOOK5	BCLK_ITP#	O	processor
43	VCC_OBS_AB	VCCP Voltage of the processor	I		44	VCC_OBS_CB	VCCP Voltage of the processor	I	
45	HOOK2	CFG[0]	O	processor 46	45	HOOK6/RESET#	RESET#	I	processor
47	HOOK3	VR_READY/SLVS_PWROK	O	System 48	47	HOOK7/DBR#	DBR#	O	processor
49	GND	GND	NA		50	GND	GND	NA	
51	SDA1	SDA	I/O	system 52	51	TD0	TD0	I	processor
53	SCL1	SCL	I/O	system 54	53	TRSTn	TRST#	O	processor
55	TCK1	Open	NA		56	TDI	TDI	O	processor
57	TCK0	TCK	O	processor 58	57	TMS	TMS	O	processor
59	GND	GND	NA		60	GND	GND (or VDD_PRESN <sup>†</sup> if required)	NA	

length ( i.e., if total pin to pin length is 6" then the LA pads

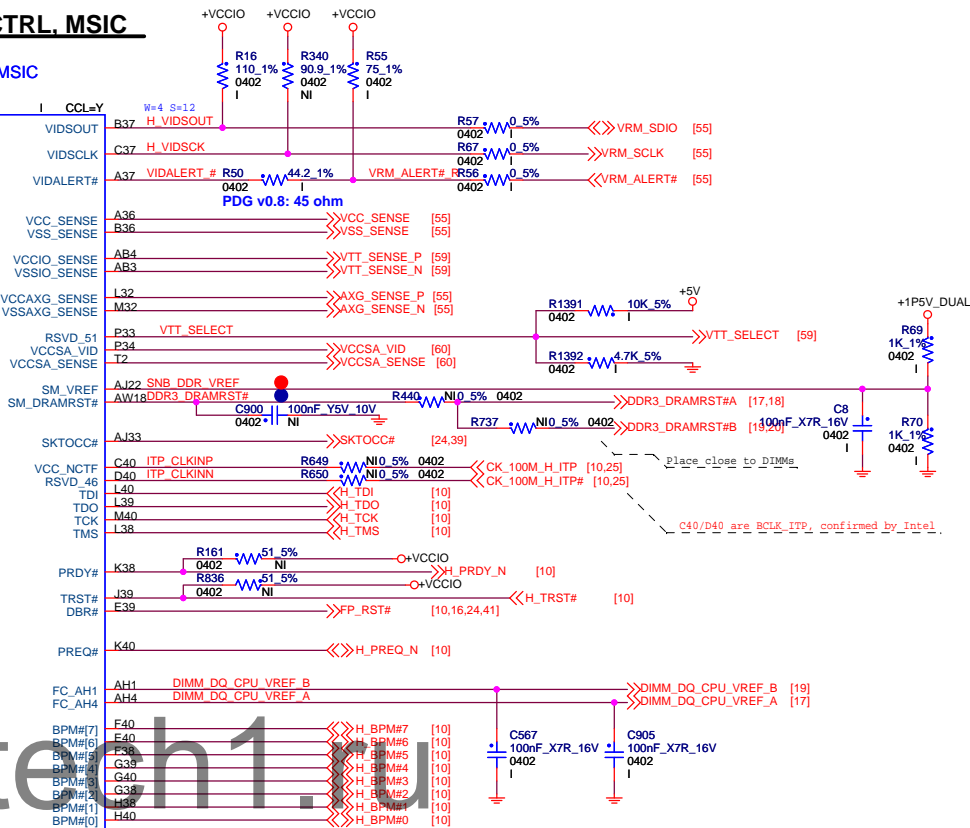
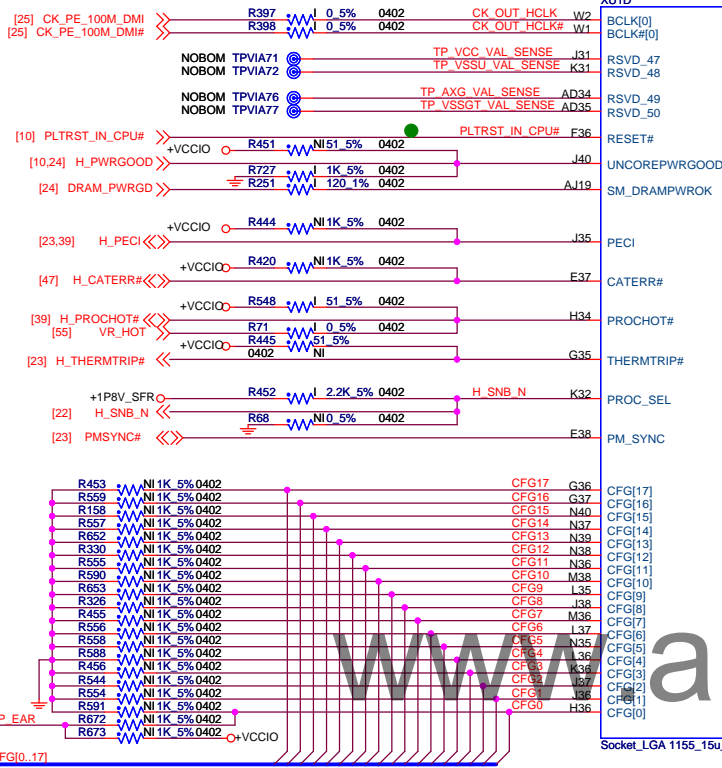
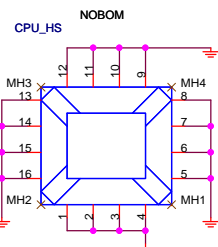
Diagram illustrating the pin connections for the Header 2X12\_DMI BOTTOM (U1) connector. The connector is labeled U1 and NI. The pins are arranged in two columns: A1-A12 on the left and B1-B12 on the right. The connections are as follows:

- Pin A12 connects to DMI\_PCH\_CPU\_RXN2 [13,21].
- Pin A11 connects to DMI\_PCH\_CPU\_RXP2 [13,21].
- Pin A10 connects to DMI\_PCH\_CPU\_RXN0 [13,21].
- Pin A9 connects to DMI\_PCH\_CPU\_RXP0 [13,21].
- Pin A8 connects to DMI\_PCH\_CPU\_RXN1 [13,21].
- Pin A7 connects to DMI\_PCH\_CPU\_RXP1 [13,21].
- Pin A6 connects to DMI\_PCH\_CPU\_RXN2 [13,21].
- Pin A5 connects to DMI\_PCH\_CPU\_RXP2 [13,21].
- Pin A4 connects to DMI\_PCH\_CPU\_RXN0 [13,21].
- Pin A3 connects to DMI\_PCH\_CPU\_RXP0 [13,21].
- Pin A2 connects to DMI\_PCH\_CPU\_RXN1 [13,21].
- Pin A1 connects to DMI\_PCH\_CPU\_RXP1 [13,21].
- Pin B12 connects to DMI\_PCH\_CPU\_RXN3 [13,21].
- Pin B11 connects to DMI\_PCH\_CPU\_RXP3 [13,21].
- Pin B10 connects to DMI\_PCH\_CPU\_RXN1 [13,21].
- Pin B9 connects to DMI\_PCH\_CPU\_RXP1 [13,21].
- Pin B8 connects to DMI\_PCH\_CPU\_RXN1 [13,21].
- Pin B7 connects to DMI\_PCH\_CPU\_RXP1 [13,21].
- Pin B6 connects to DMI\_PCH\_CPU\_RXP3 [13,21].
- Pin B5 connects to DMI\_PCH\_CPU\_RXN3 [13,21].
- Pin B4 connects to DMI\_PCH\_CPU\_RXN3 [13,21].
- Pin B3 connects to DMI\_PCH\_CPU\_RXN1 [13,21].
- Pin B2 connects to DMI\_PCH\_CPU\_RXN1 [13,21].
- Pin B1 connects to DMI\_PCH\_CPU\_RXP1 [13,21].

Ground connections are shown at the bottom of the connector.

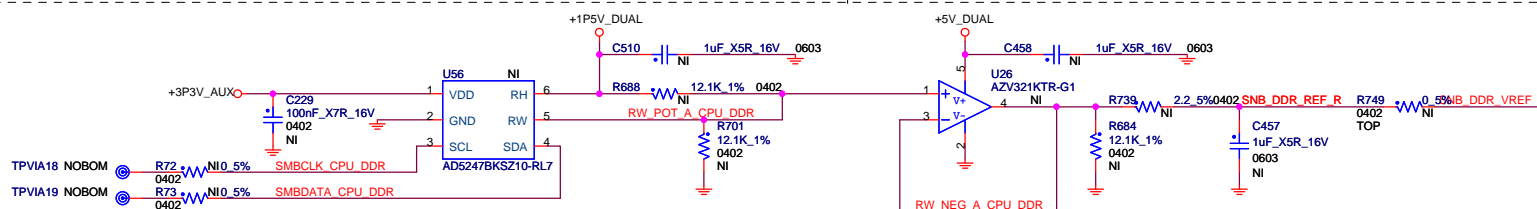
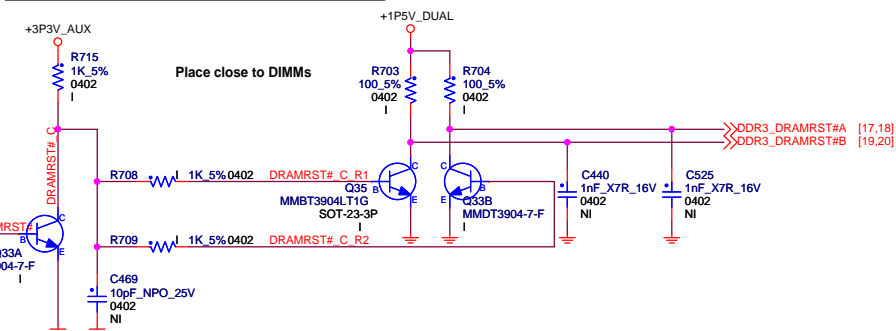
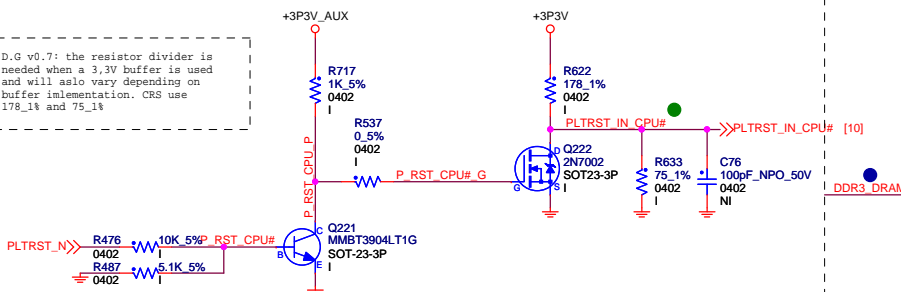
		Hon Hai Precision Industry Co. Ltd.	
<b>Foxconn CMMSG</b> Foxconn WuHan China		Phone: 755-28128988 Ext.22260 Fax: +86-755-2812-8988	
Title <b>Intel XDP Debugging Connector / DMI debug header</b>			
Size Custom	Document Number <b>IS6XM uATX</b>		Rev <b>X7</b>
Page Modified: Wednesday, March 02, 2011		08:28:00 (UTC/GMT)	Sheet 10 of 65


## MCP-VID,CTRL,MSIC



```
DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP
```

Ensure timings and edge rates are met on PLTRST# going to processor.

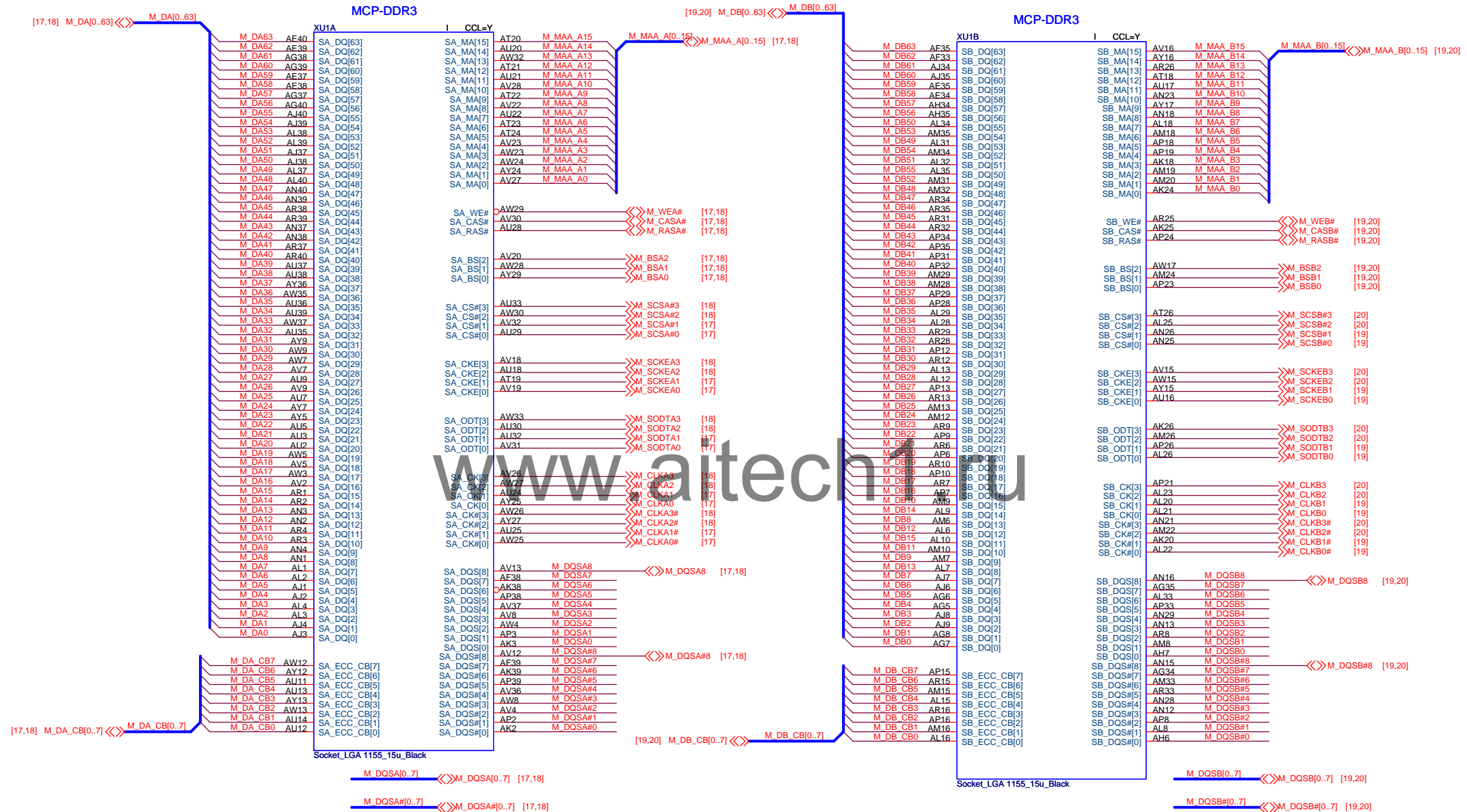


		Hon Hai Precision Industry Co. Ltd.	
<b>Foxconn CMMSG</b> Foxconn Wuhan China		Phone: 755-28128988 Ext.22260 Fax: +86-755-2812-8988	
Title <b>MCP - CLK, CTRL, MISC, DEBUG</b>			
Size Custom	Document Number <b>IS6XN uATX</b>	Rev <b>X7</b>	
Page Modified: Wednesday, March 02, 2011		09:21:34 (UTC+08)	Sheet 11 of 65



## MCP - DDR3 CH-A

## MCP - DDR3 CH-B



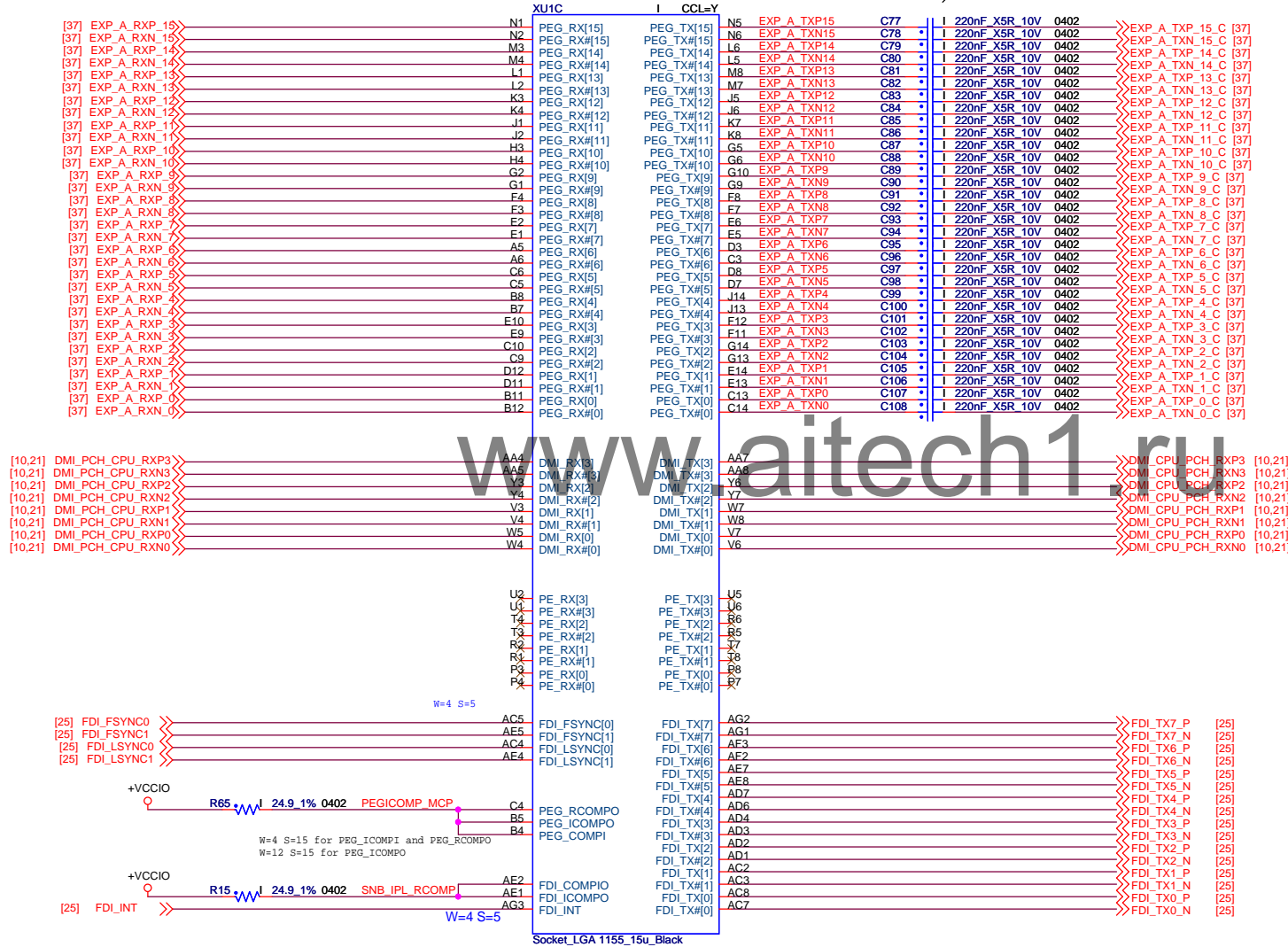


Routing bundles are differential pairs that share a common equalization register. Differential pair 0 and 1 are a bundle, differential pair 2 and 3 are a bundle, and so on. For example on PCIE: PEG\_TX\_#0 and PEG\_TX\_#1 or PEG\_TX\_#2 and PEG\_TX\_#3 are two examples. Length match pairs in a bundle to within 0.4 inch.

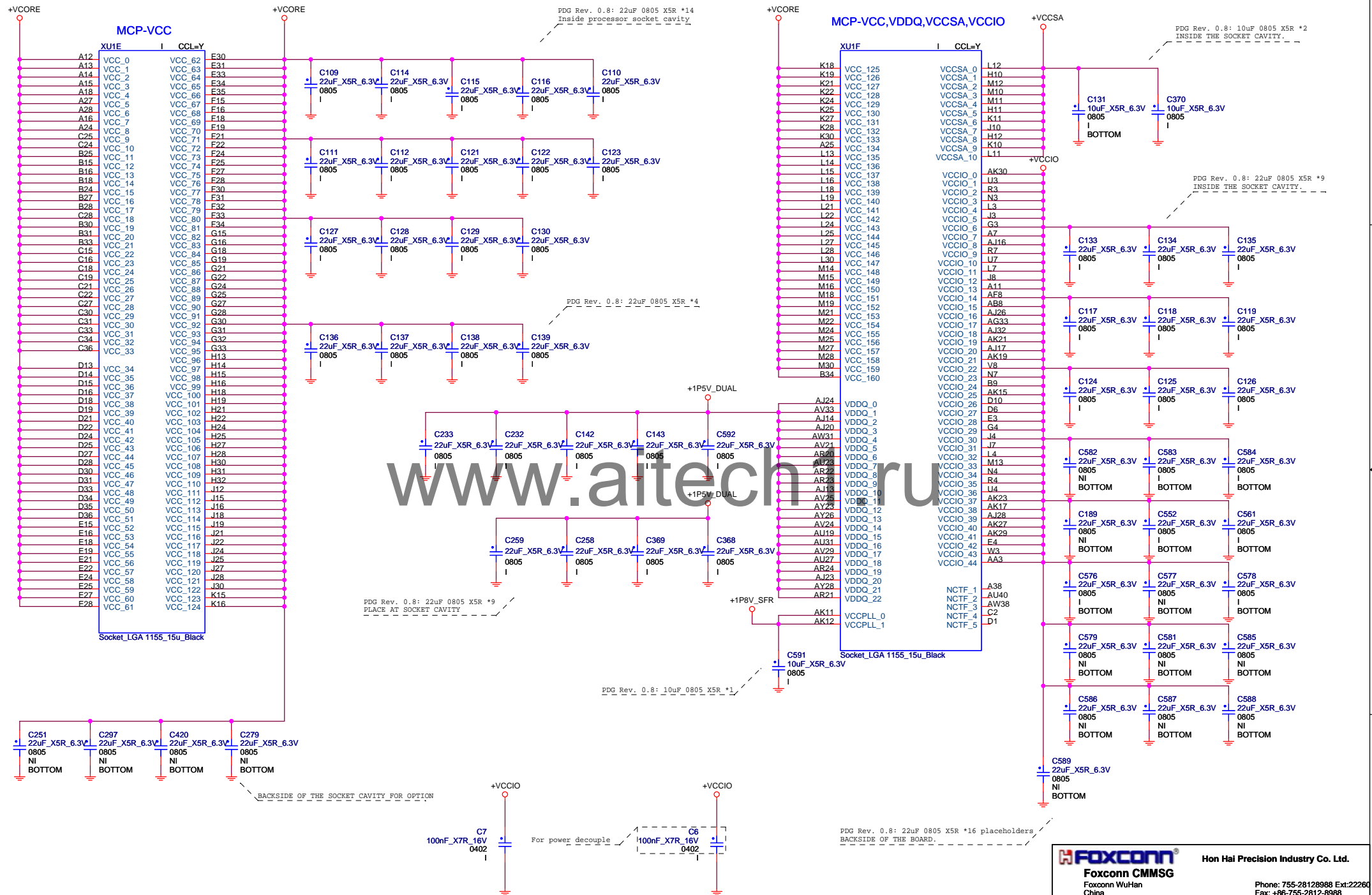
## MCP - PCIE,DMI,FDI

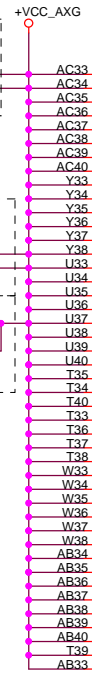
### MCP-PEG,PE,DMI,FDI

PDG v0.8: 180nF ~ 265nF

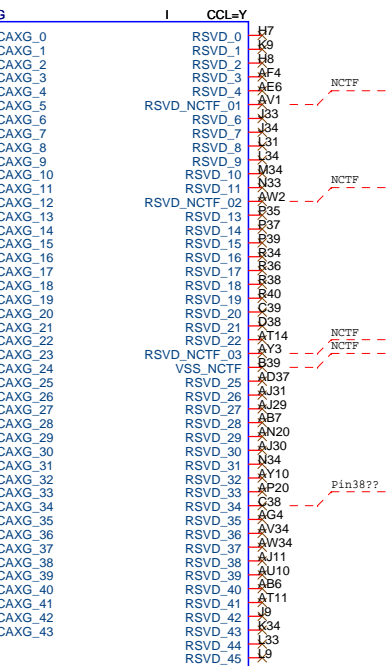


SHORT B4 & C4 TOGETHER, ROUTE AS A SINGLE 4 MIL TRACE TO R65.  
ROUTE B5 TO R65 AS A SEPERATE 12 MIL TRACE

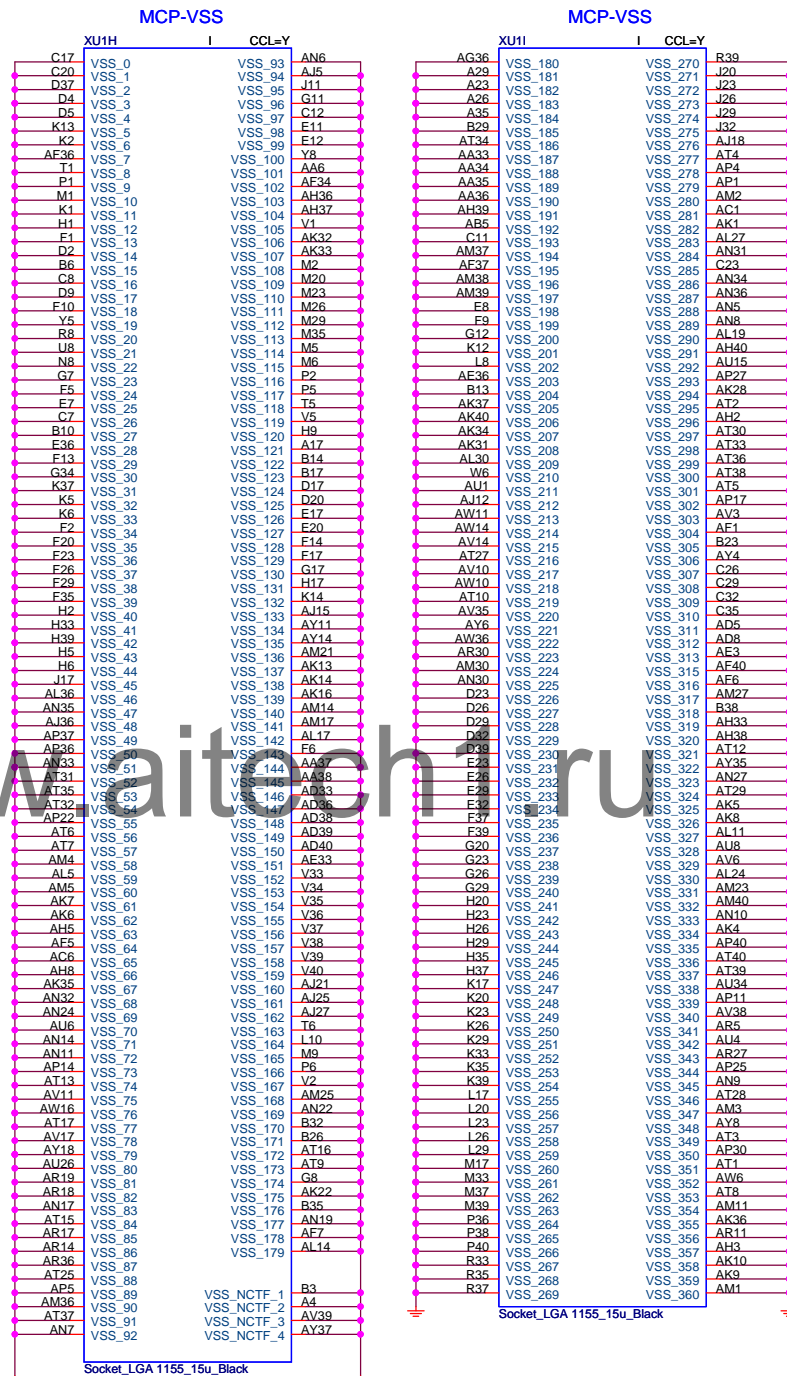




Socket LGA 1155 15u Black



Address	Disassembly	Comment
A136	VSS_48	VSS_141
AP37	VSS_49	VSS_142
AP36	VSS_50	F6
AN33	VSS_51	AA97
AT35	VSS_52	AA38
AT36	VSS_53	AD33
AT32	VSS_54	AD36
AP22		AD38



Socket\_LGA 1155\_15u\_Black

## Intel PCH Debugging Connector

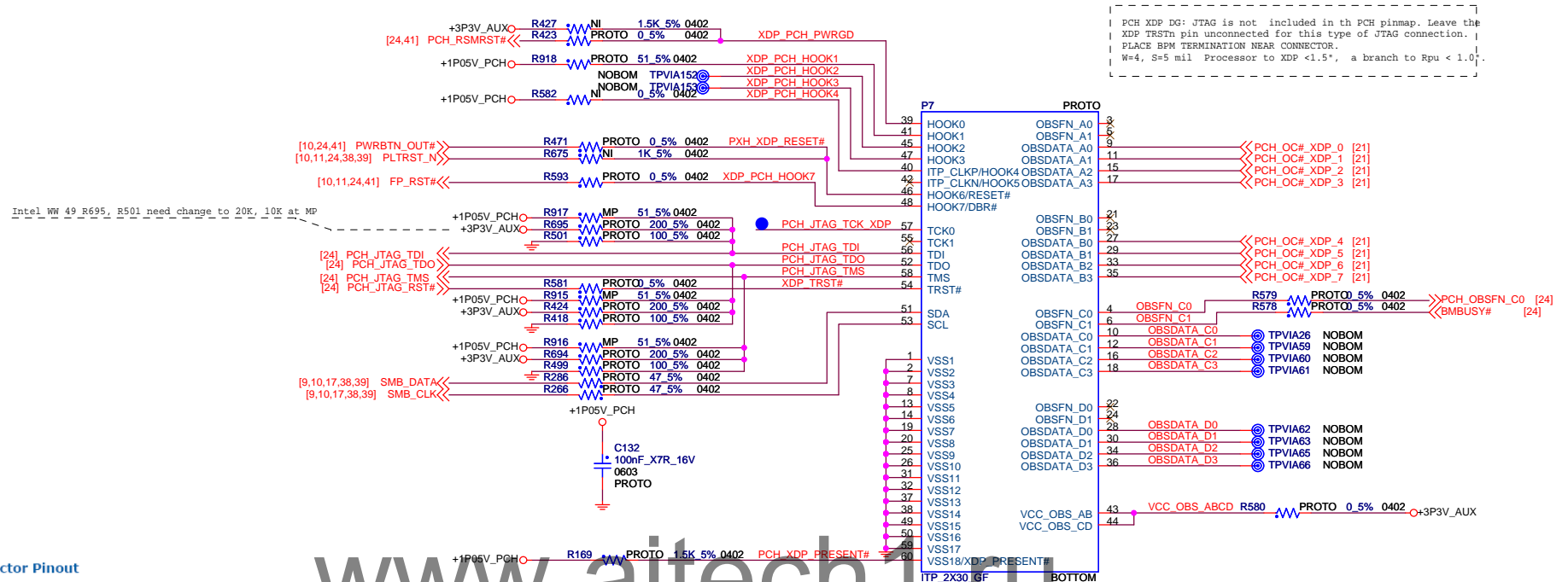


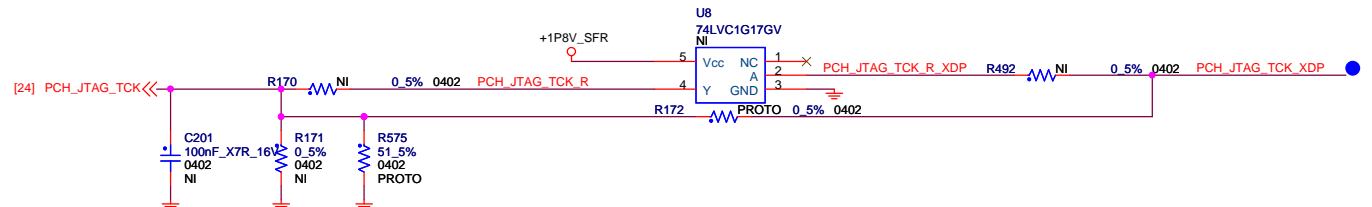
Table 4-1. PCH XDP Connector Pinout

Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	GND	GND	NA		4	GND	GND	NA	
3	OBSFN_A0	Open	NA		2	OBSFN_C0	GPI015	1	PCH
5	OBSFN_A1	Open	NA		6	OBSFN_C1	BMBUSY# / GPI00	1	PCH
7	GND	GND	NA		8	GND	GND	NA	
9	OBSDATA_A0	OC0# / GPIO59	1	PCH	10	OBSDATA_C0	MGP107 / GPIO28	1	PCH
11	OBSDATA_A1	OC1# / GPIO40	1	PCH	12	OBSDATA_C1	GPI035	1	PCH
13	GND	GND	NA		14	GND	GND	NA	
15	OBSDATA_A2	OC2# / GPIO41	1	PCH	16	OBSDATA_C2	SATA0GP / GPIO21	1	PCH
17	OBSDATA_A3	OC3# / GPIO42	1	PCH	18	OBSDATA_C3	SATA1GP / GPIO19	1	PCH
19	GND	GND	NA		20	GND	GND	NA	
21	OBSFN_B0	Open	NA		22	OBSFN_D0	Open	NA	
23	OBSFN_B1	Open	NA		24	OBSFN_D1	Open	NA	
25	GND	GND	NA		26	GND	GND	NA	
27	OBSDATA_B0	OC4# / GPIO43	1	PCH	28	OBSDATA_D0	SATA2GP / GPIO16	1	PCH
29	OBSDATA_B1	OC5# / GPIO9	1	PCH	30	OBSDATA_D1	SATA3GP / GPIO37	1	PCH
31	GND	GND	NA		32	GND	GND	NA	
33	OBSDATA_B2	OC6# / GPIO10	1	PCH	34	OBSDATA_D2	SATA4GP / GPIO16	1	PCH
35	OBSDATA_B3	OC7# / GPIO14	1	PCH	36	OBSDATA_D3	SATA5GP / GPIO49	1	PCH
37	GND	GND	NA		38	GND	GND	NA	
39	HOOK0	RSMRST#	1	PCH	40	ITPCLK/HOOK4	Open	NA	
41	HOOK1	BS_FWRGO_RST#	0	system	42	HOOK5	Open	NA	
43	VCC_OBS_AB	VccSus3_3	NA		44	VCC_OBS_CD	VccSus3_3	NA	
45	HOOK2	Open	1		46	HOOK6 / RESET#	RSMRST#	1	PCH
47	HOOK3	Open	NA		48	HOOK7/DBR#	SYS_RESET#	0	PCH
49	GND	GND	NA		50	GND	GND	NA	
51	SDA	SDA	I/O	system	52	TDO	JTAG_TDO	1	PCH
53	SCL	SCL	I/O	system	54	TRSTn	Open	NA	
55	TCR1	Open	NA		56	TDI	JTAG_TDI	0	PCH
57	TCR0	JTAG_TCK	0	PCH	58	TMS	JTAG_TMS	0	PCH
59	GND	GND	NA		60	GND	GND (or XDP_PRESN T# if required)	NA	

In Subject: Ibox peak JTAG requirements

In addition to the changes shown in the WW35 MOW Intel recommends customers implement the changes below on their platforms to support JTAG debug and boundary scan capabilities. These changes will be reflected in future CRB schematics and the Debug Port Design Guide.

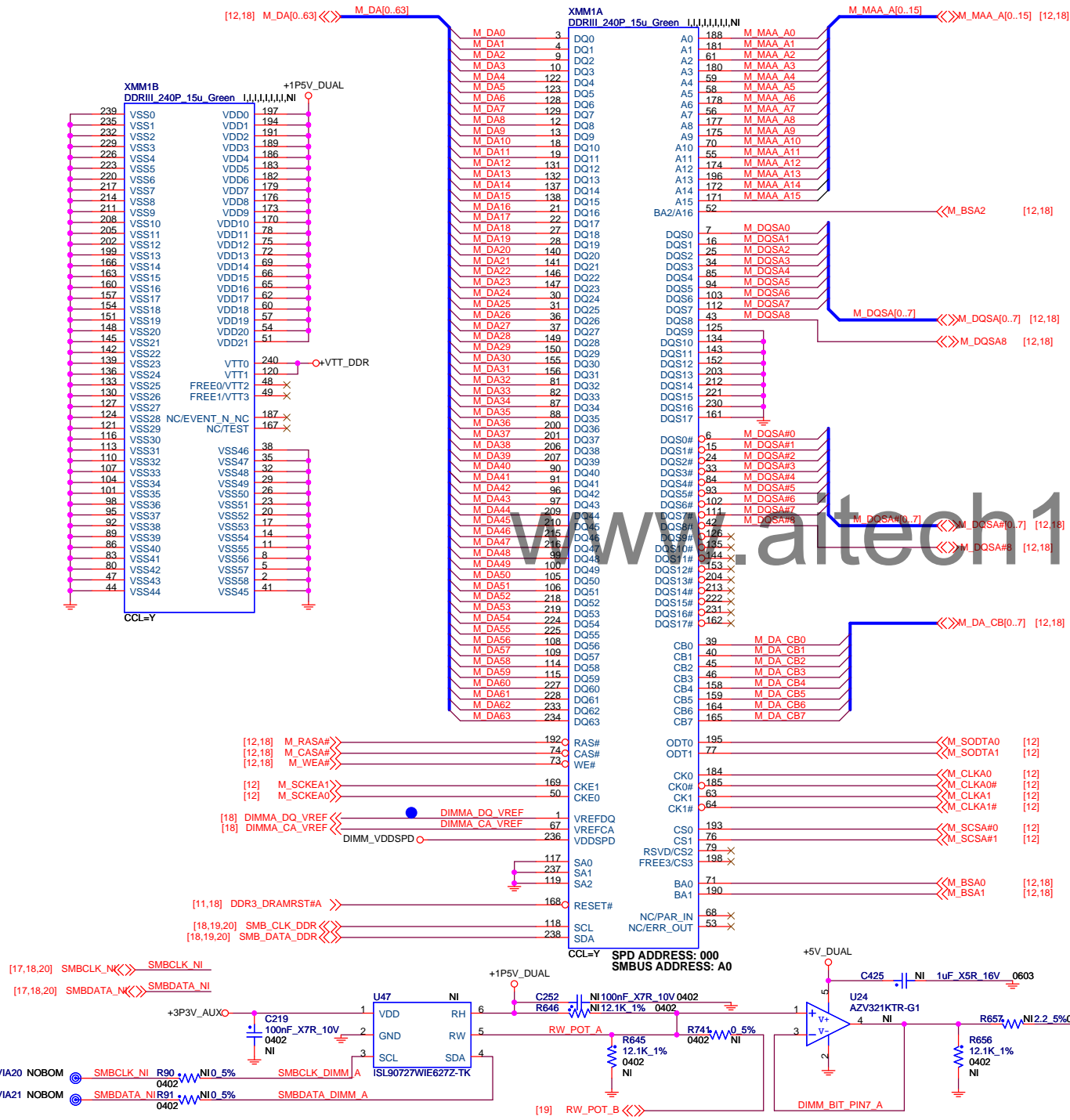
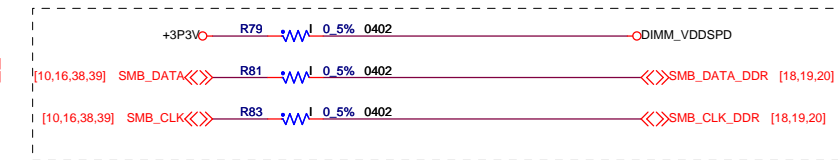
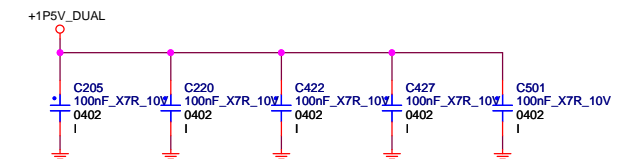
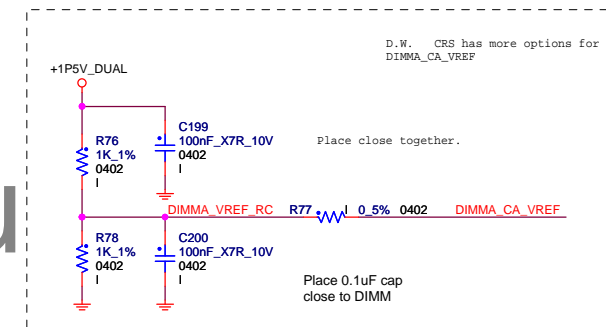
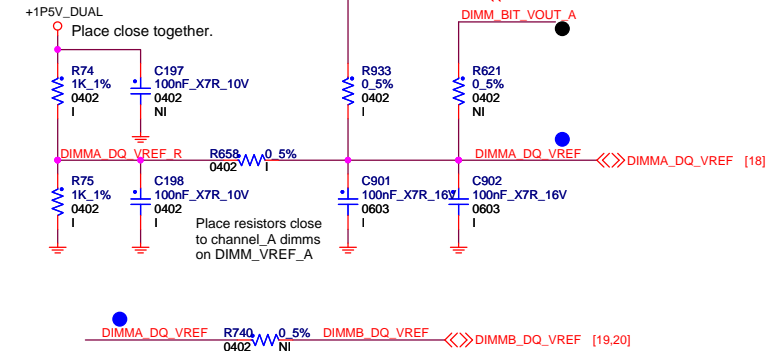
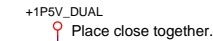
- a) JTAG\_TDI, JTAG\_TDO, JTAG\_TMS, TRST# require a strong pull-ups to a 1.05V.
- a) Pre-production and/or development systems should be connected to a 1.05 V sus rail, or Thevenin equivalent derived from 3.3 V sus. This connection will insure Intel supported debug is functional, however it will draw power in Sx states and thus is not recommended for production
- b) Production systems should include a 51 ohm pull-up to 1.05 Core. In this configuration power draw in Sx states is minimized, and JTAG boundary Scan is functional. However, Intel supported debug via this interface is. Production layouts should include sites for connection to a 1.05V sus rail, but components should not be stuffed.
- c) Intel recommends JTAG\_TDO have a placeholder pull-up to 1.05V sus and core rails. The pull-up resistor pads should be left un-stuffed for ES1 due to an issue where JTAG\_TDO will drive 3.3V signaling level instead of 1.05V.



DIMM Slot Sequence from MCP:

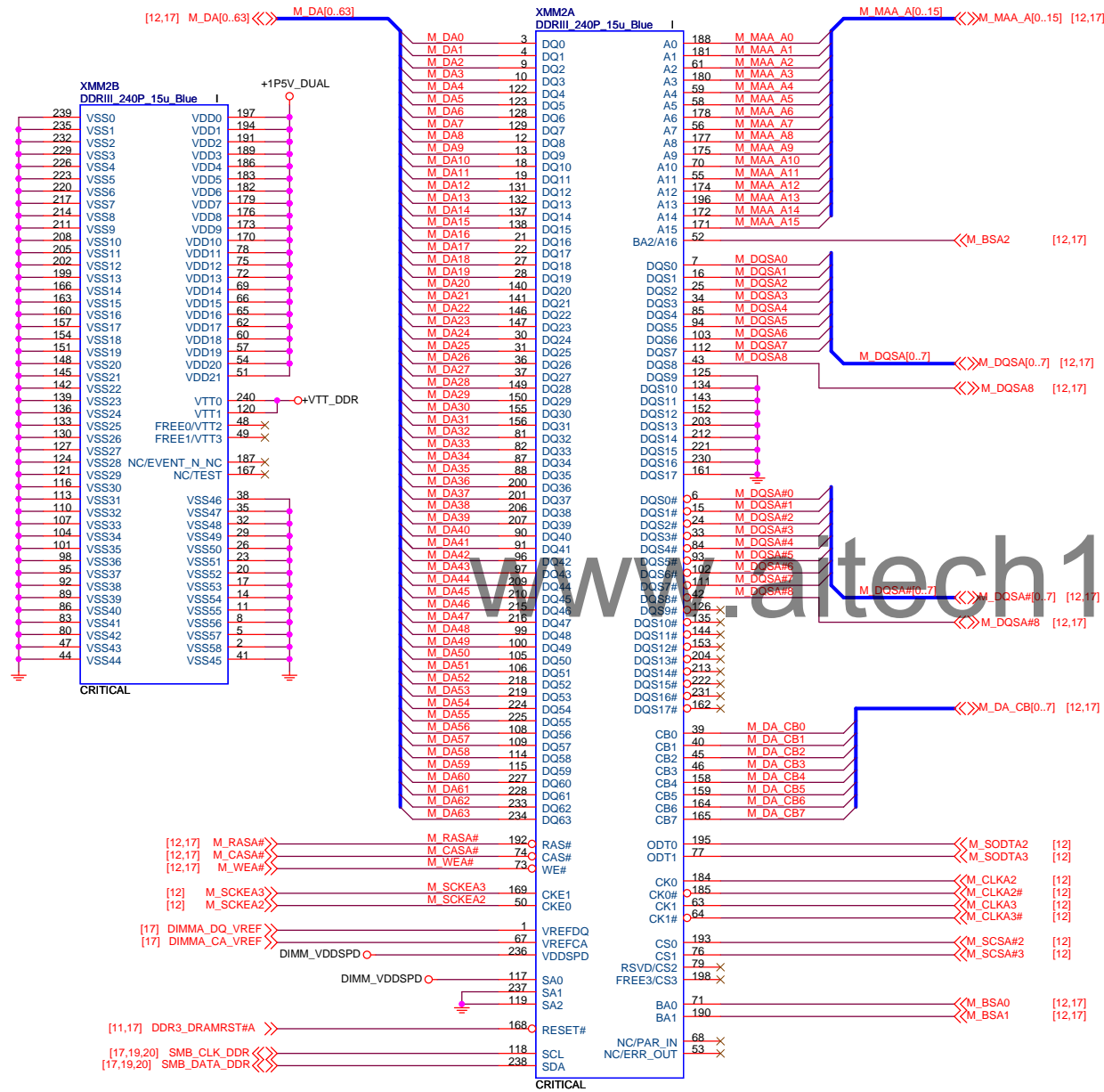
- CHA DIMM0 ( XMM1)
- CHA DIMM1( XMM2)
- CHB DIMM0(XMM3)
- CHB DIMM1(XMM4).

Memory module install rule: furthest slot from CPU is the 1st, then closest slot





DDR3\_CHA\_DIMM1 Socket Color: Green  
2nd DIMM slot from MCP

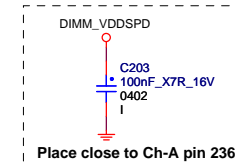
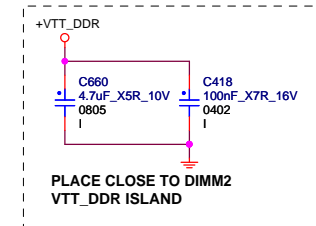


```

DIMM Slot Sequence from MCP:
- CHA DIMM0 ( XMM1)
- CHA DIMM1( XMM2)
- CHB DIMM0(XMM3)
- CHB DIMM1(XMM4).

Memory module install rule: furthest slot from CPU is the 1st, then closest slot.

```

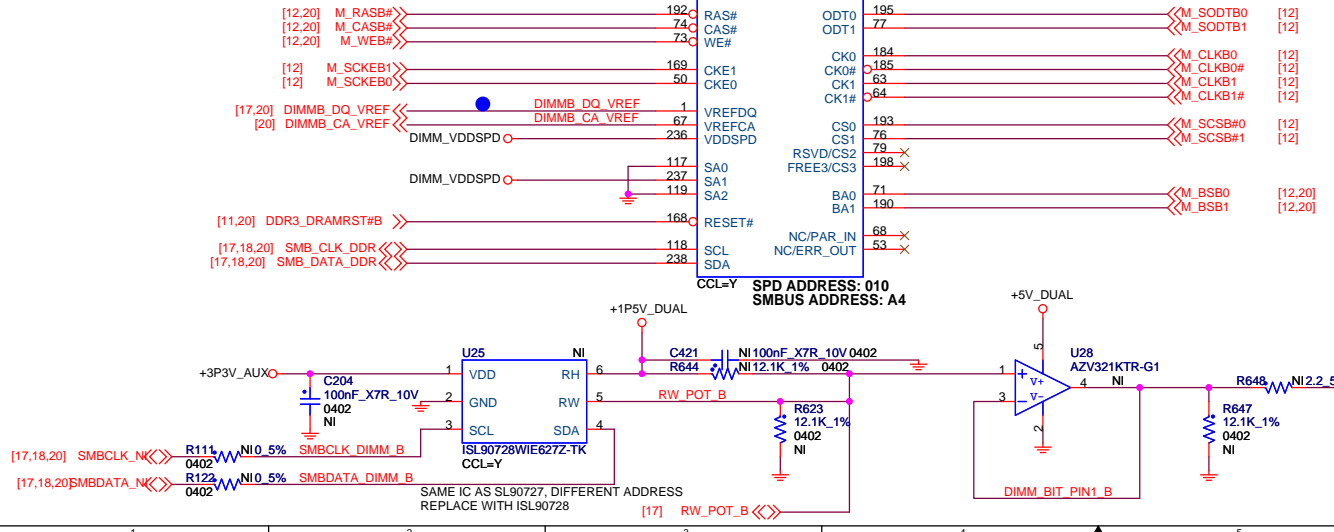
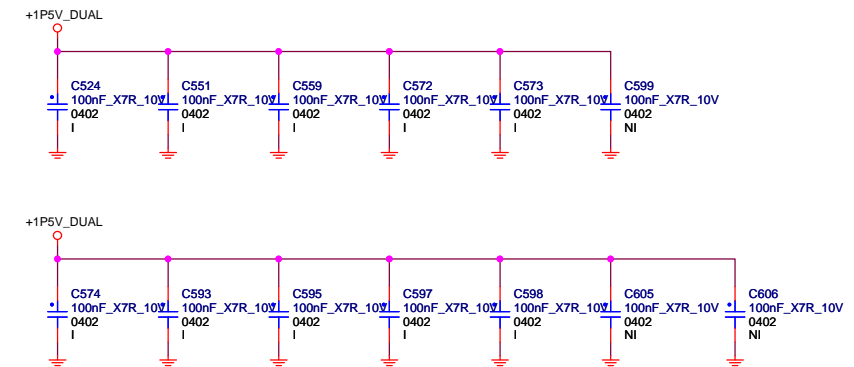
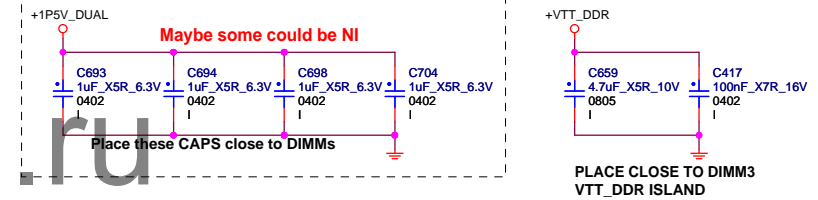
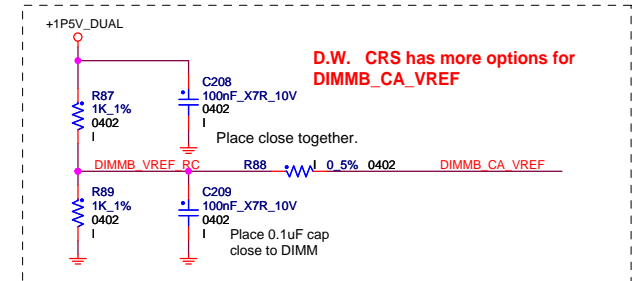
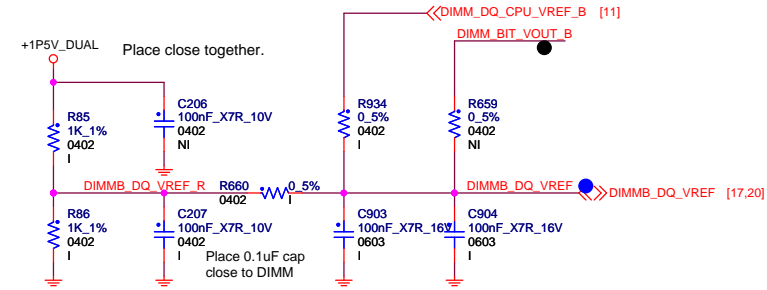
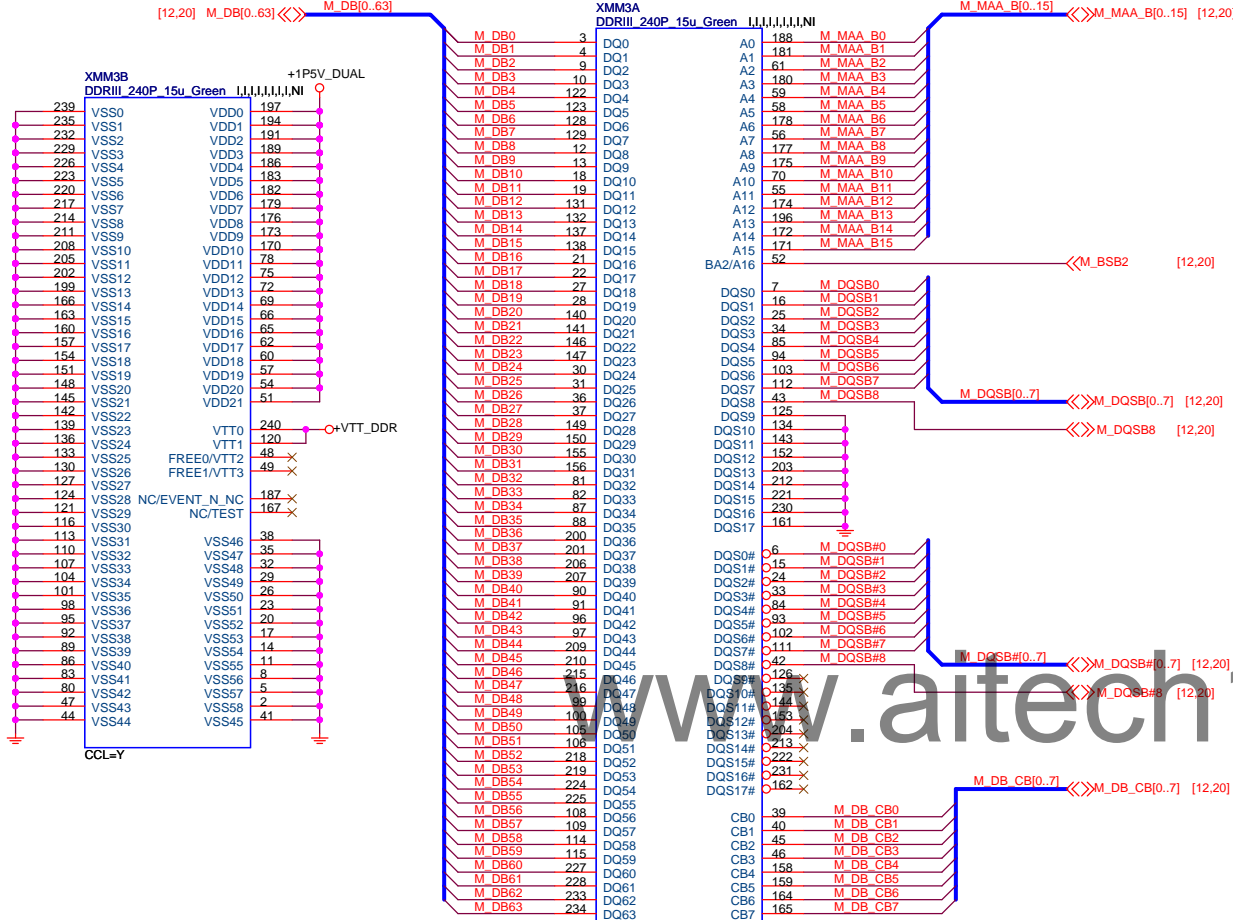


SPD ADDRESS: 001  
SMBUS ADDRESS: A2

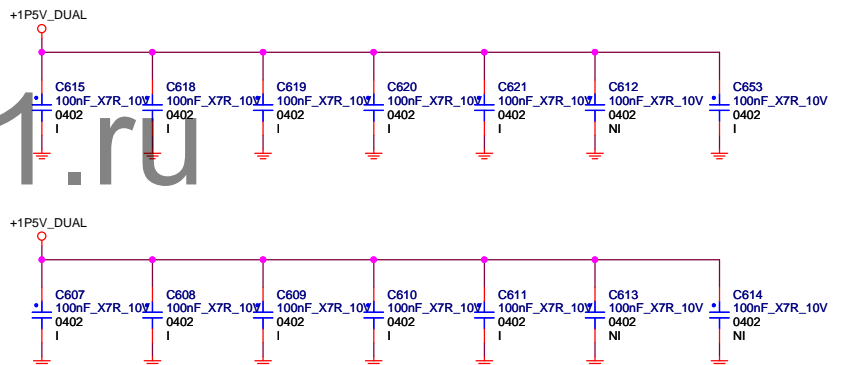
# DDR3 CHB DIMM Socket Color: Blue 3rd DIMM slot from MCP


DIMM Slot Sequence from MCP: CHA DIMM0 ( XMM1), CHA DIMM1( XMM2), CHB DIMM0(XMM3), CHB DIMM1(XMM4).

Memory module install rule: furthest slot from CPU is the 1st, then closest slot.



**Memory module install rule: furthest slot from CPU is the 1st, then closest slot.**



		Hon Hai Precision Industry Co. Ltd.	
<b>Foxconn CMMSG</b> Foxconn WuHan China		Phone: 755-28128988 Ext:22260 Fax: +86-755-2812-8988	
Title <b>DDR3 CH-B DIMM2</b>			
Size Custom	Document Number <b>IS6XM uATX</b>		Rev <b>X7</b>
Page Modified: Wednesday, March 02, 2011		09:21:36 (UTC/GMT)	Sheet 20 of 65



The probing point requires populating a resistor stuffing option that can be used to break the path to the device very near the device pins and ideally terminate each line (TX+/TX-) to ground through a 50 Ohms 1% resistor. Also, an AC coupling capacitor is required near the device pins. The resistor package/footprint must be as small as possible, preferably size 0402. The population of a 50-Ohm resistor, as shown in Figure 4-5,

It is highly recommended to have DMI on surfaced vias (not buried).

PDG v0.8: The DMI compensation pins should be tied together and connected to the PCH 1.05V rail (Vcc1\_05\_Filter) via a 49.9 ohm, 1% resistor

Layout Note:  
PLACE CLOSE TO LAN PHY

U4B CCL=Y  
Cougar Point

Check without used??

USB ports 6 and 7 are disabled on 12 port SKU's.  
(B65)

No longer than 450 mils  
W=4 S=15

OC# [4:7] can only be used  
for EHCI Controller 2

OC# [3:0] can only be used  
for EHCI Controller 1

USB ports 6 and 7 are disabled on 12 port SKU's. (B65)

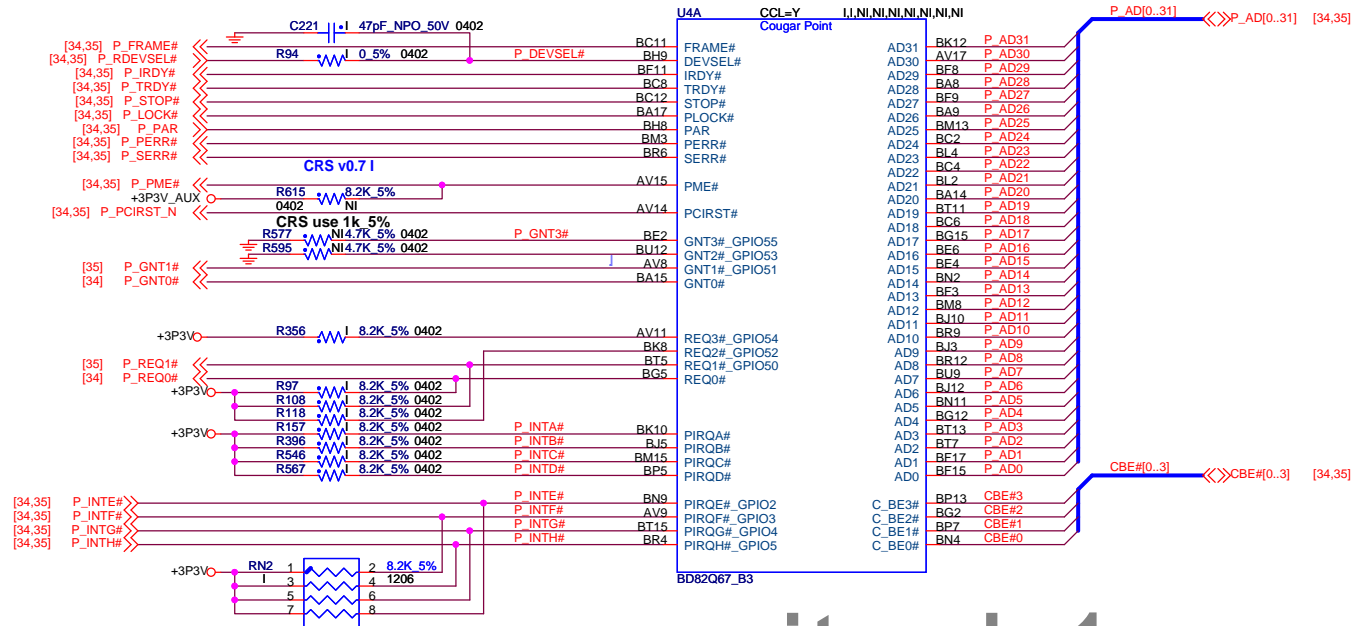
EHCI 1# Port 0-7  
EHCI 2# Port 8-13

NOTES:

1. OC# pins are not 5 V tolerant.
2. OC# pins must be shared between ports
3. OC# [3:0] can only be used for EHCI Controller 1
4. OC# [4:7] can only be used for EHCI Controller 2

EHCI#1: Device 29 Function 0; EHCI#2 Device 26 Function 0  
Port 0-Port7: EHCI1 Port0 RMH1  
Port 8-Port13: EHCI2 Port0 RMH2

## PCH - PCI



**GNT3: TOP-BLOCK SWAP OVERRIDE INTERNAL PULL UP 20K**  
A weak internal pull up, disabled after PLTRST# deasserts. A16 SWAP  
OVERRIDE: OVERRIDE IF SAMPLED LOW

**GNT2: EST strap for server only. Do not pull low**

BOOT DEVICE	GNT1#	SATA1GP/GPIO19
LPC	0	0
PCI	1	0
SPI (Default)	1	1

**GNT1#:** has a weak internal pull up, 20k.  
**SATA1GP:** has a weak internal pull up, TBD..

**PDG V0.7 check list:**

Default (SPI):

Left both SATA1GP/GPIO19 and GNT0# floating. No pull up required.

Boot from PCI:

Connect GNT0# to ground with 1k Ohm pull-down resistor.

Leave SATA1GP/GPIO19 Floating.

Boot from LPC:

Connect both SATA1GP/GPIO19 and GNT0# to ground with 1k Ohm pull-down resistor.

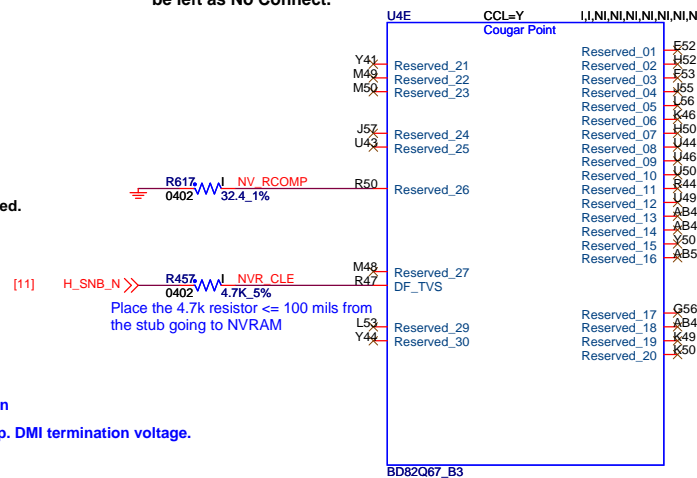
**EDS v0.5 page 70: NV\_CLE has a weak internal pull up**

**EDS v0.5 page 77: NV\_CLE / NV\_ALE has a 20 k internal pull down**

**PDG v0.7 check list page 379: NV\_CLE has a weak internal pull up. DMI termination voltage.**

For future processor compatibility, the PROC\_SEL should be connected to the NV\_CLE pin on the PCH through an isolation resistor of 4.7k ohm and a 2.2k ohm pull up to V\_NAND\_IO. Place the 4.7k resistor <= 100 mils from the stub going to NVRAM connector. Refer Figure 5-4 below for implementation

**PDG:** If not implemented, the dual channel NAND interface signals, including NV\_RCOMP, can be left as No Connect.



## PCH - NVRAM

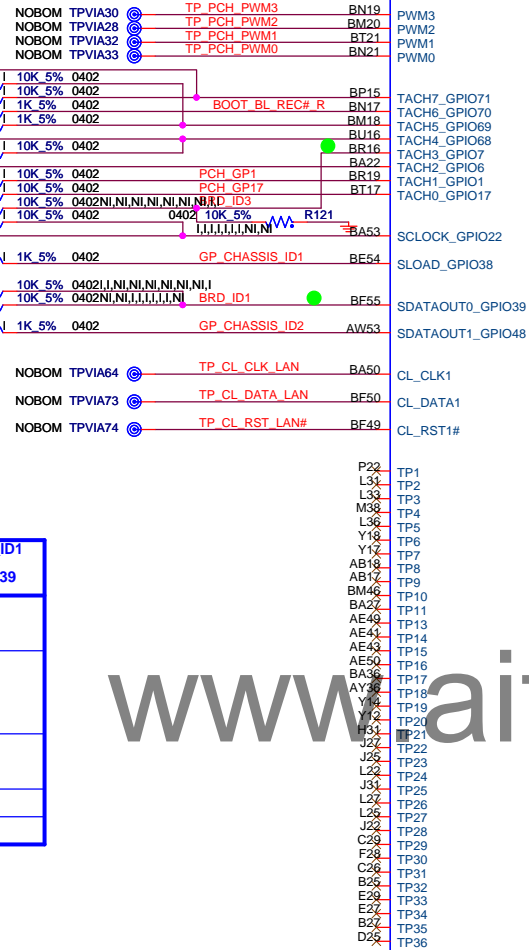
Non-Pull-up have serial 8.2K @OtherPage

The serial 1k resistor is for Current limit.

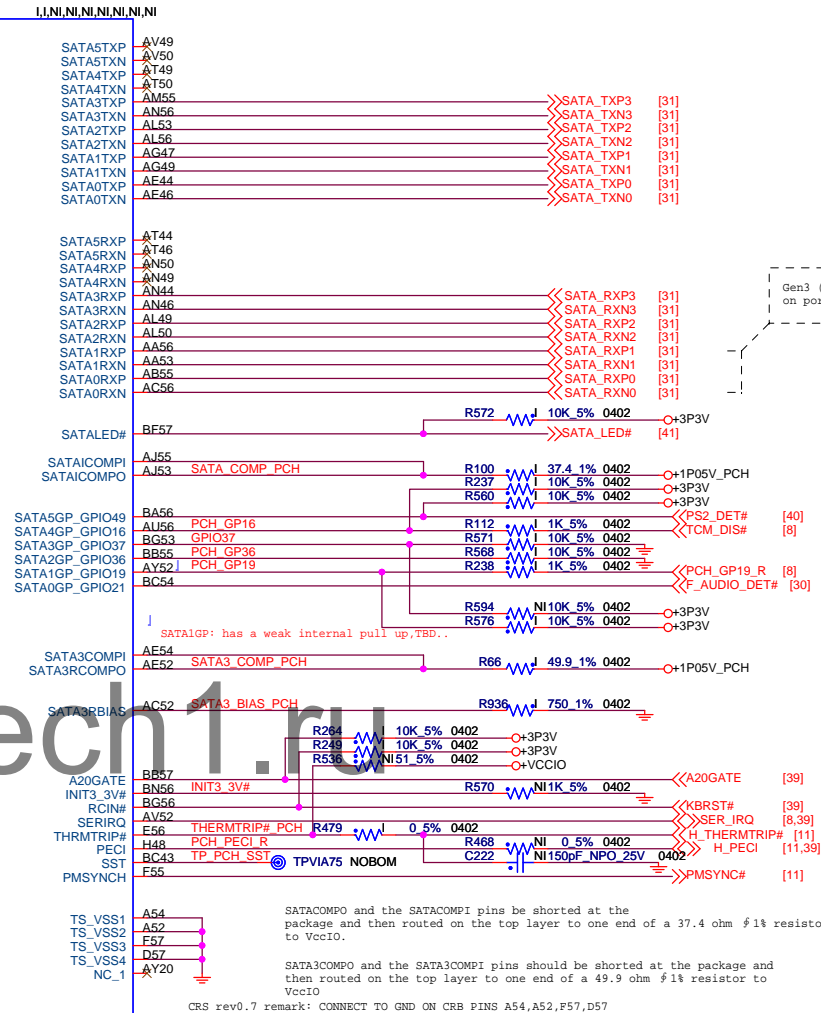
PCA Board ID [3:1]:

Project	BRD_ID3 GPIO7	BRD_ID2 GPIO35	BRD_ID1 GPIO39
Manchester-LI	0	0	0
Manchester-LC			
Ventoux-LI			
Thames-LI	0	1	1
Thames-LC			
Merton-LI			
Merton-LC	0	0	1
Edge91-LC	1	0	1
Changzhou-LC	1	0	0

SLP\_SUS# is a signal on PCH which indicate the system in deep sleep state. The deep sleep state is a lower power, limited wake features supported state where the Suspend well is powered off and only the DSW will in PCH remains powered.



BD82Q67\_B3



SATACOMPO and the SATACOMPI pins be shorted at the package and then routed on the top layer to one end of a 37.4 ohm  $\pm 1\%$  resistor to VccIO.

SATA3COMPO and the SATA3COMPI pins should be shorted at the package and then routed on the top layer to one end of a 49.9 ohm  $\pm 1\%$  resistor to VccIO

CRS rev0.7 remark: CONNECT TO GND ON CRB PINS A54,A52,F57,D57

Gen3 ( 6Gb/s ) support is on ports 0 & 1 only

SUSACK# Input. Connect to deep sleep well monitoring logic to give PCH indication that system is entering deep sleep state. May be connected directly to system supporting deep sleep well but not wishing to participate in the handshaking.

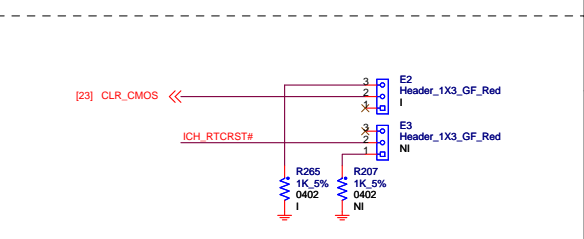
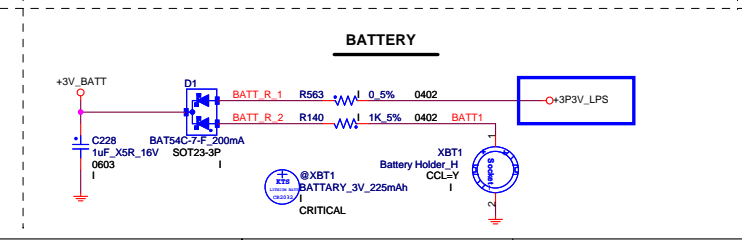
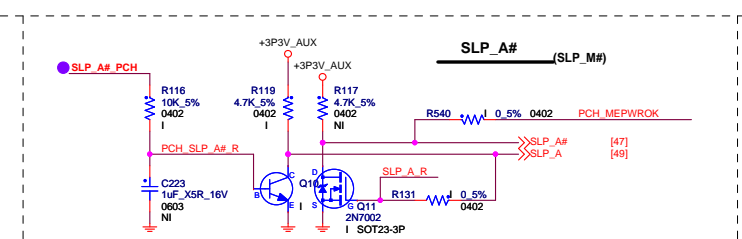
SUSWARN#/SUSPWRACK#/GPIO30/MSP101:Output. Connect to external deep sleep well control logic.May be connected directly to SUSACK# for system supporting deep sleep well but not wishing to participate in the handshaking.

SUSPWRACK#/SUSWARN#/GPIO30/MSP101: Connect to external sus well control logic to turn off sus well when it is not needed. Requires a 10 k pull up to VccSus3.3. Not needed when deep sleep is supported on the platform.

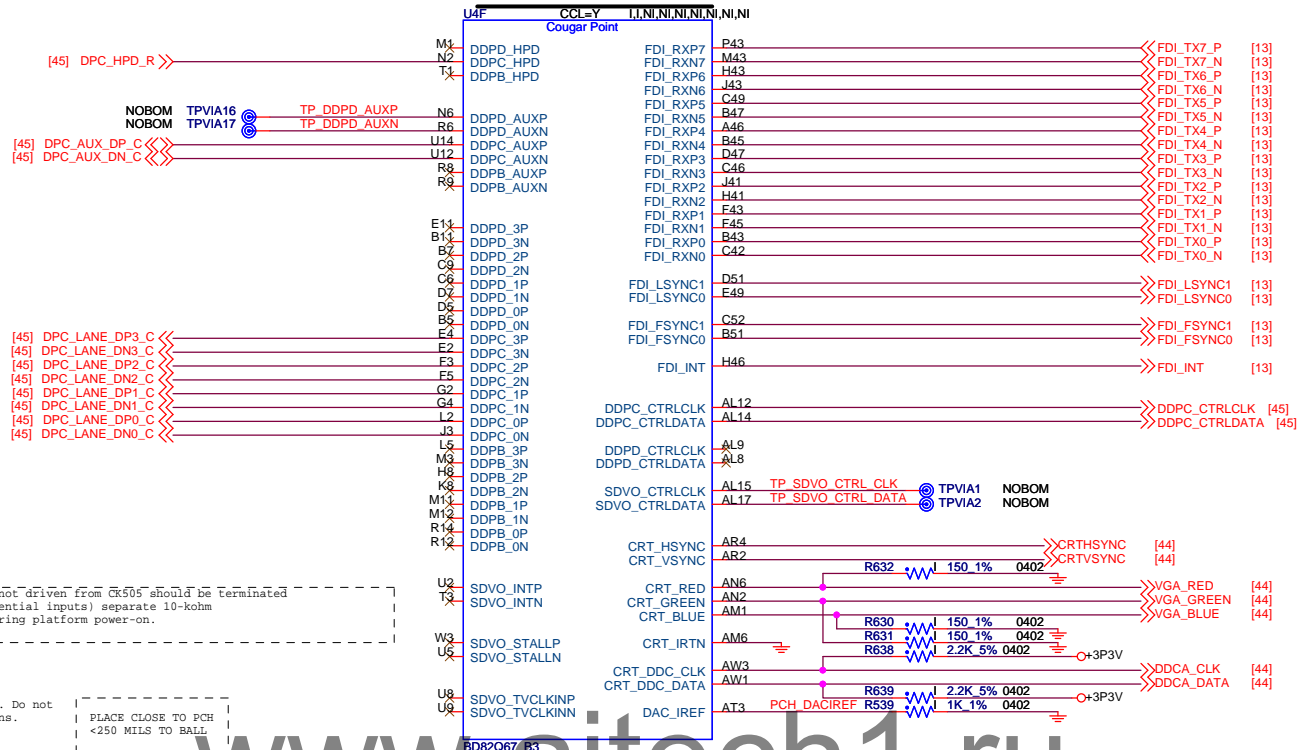
Only PCIECLKREQ[2:1]# on PCH are core well powered. All other PCIECLKREQ# are suspend well powered.

If using a Suspend well powered CLKREQ# input on PCH, platform can optionally use a blocking circuit to prevent any possible leakage path in S3-S5 states, from the external 3.3-V Suspend rail through the CLKREQ# pin on the PCIe device to the PCIe device core rails. The current blocking circuit may not be required if the PCI Express\* device allows its CLKREQ# output to be pulled up to a Suspend rail.

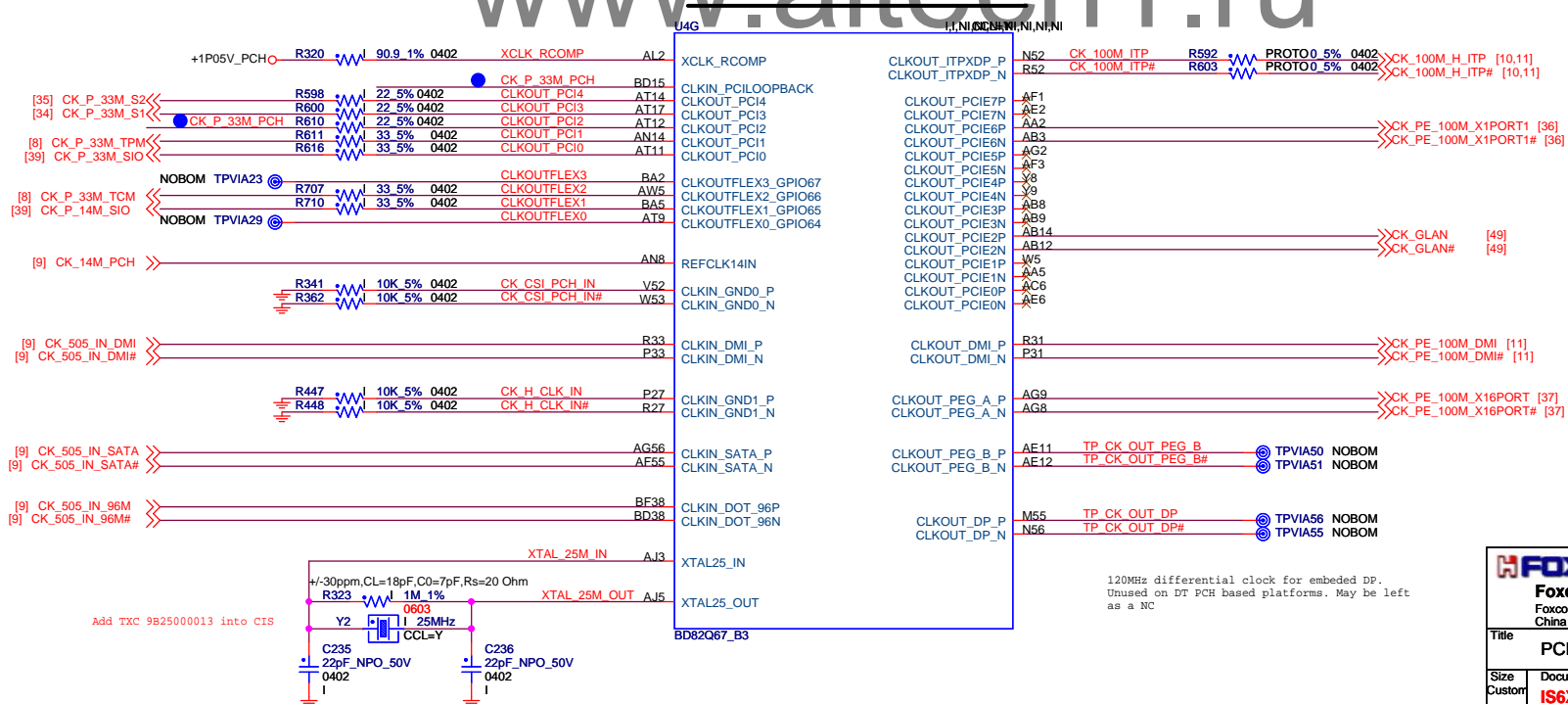
CheckList no external resistor request.



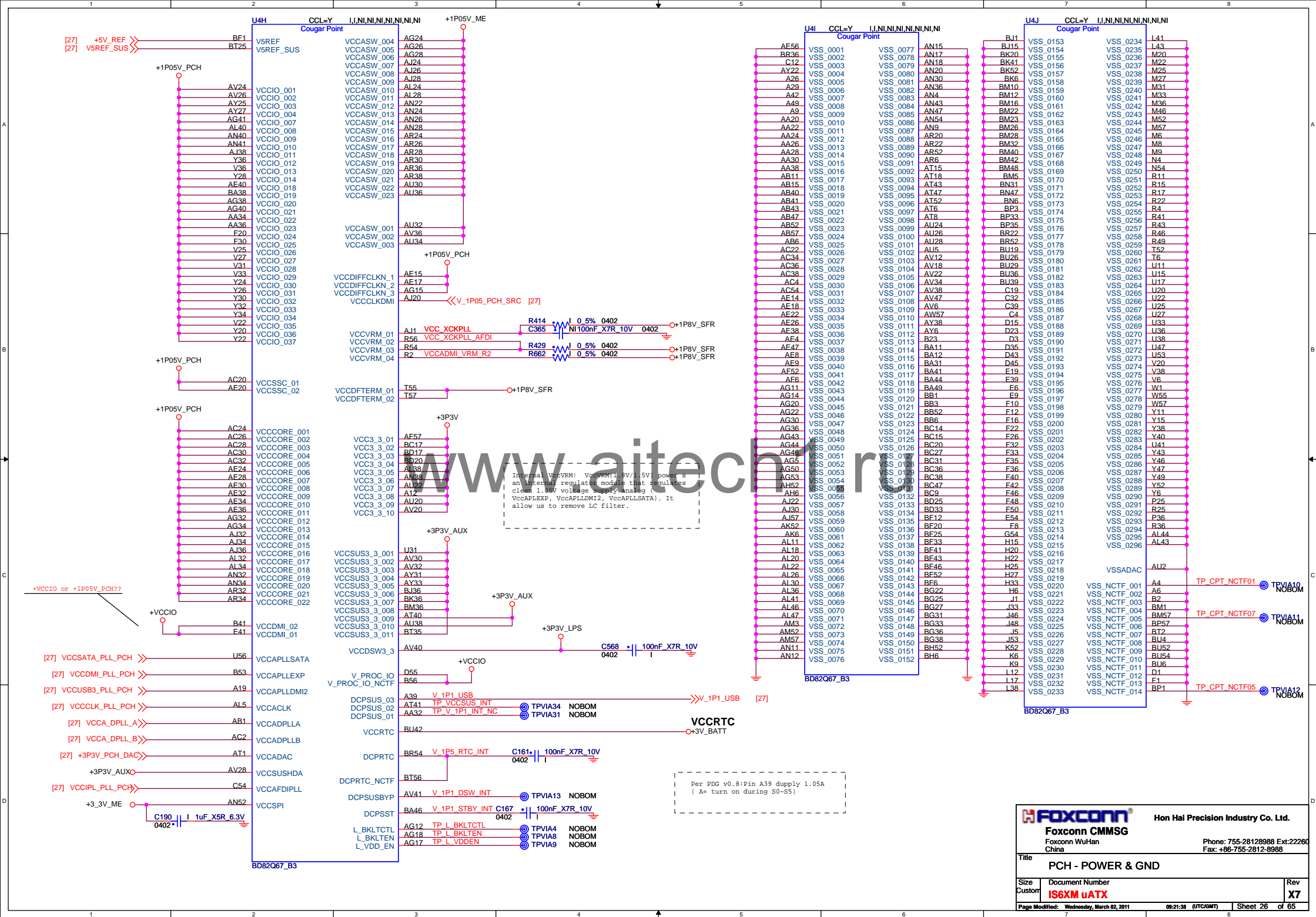
# PCH - DP AND FDI

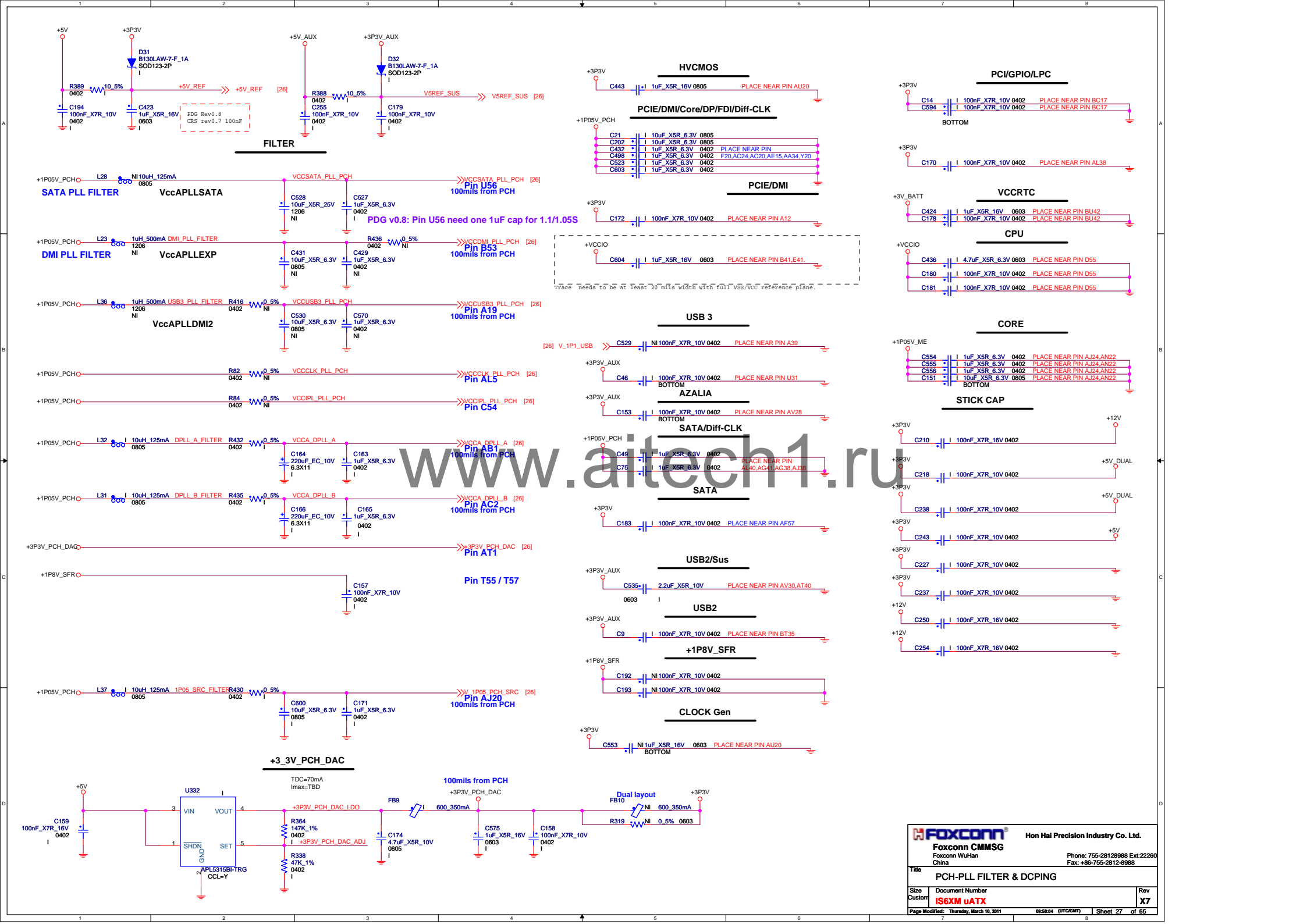


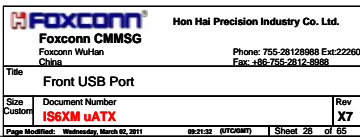
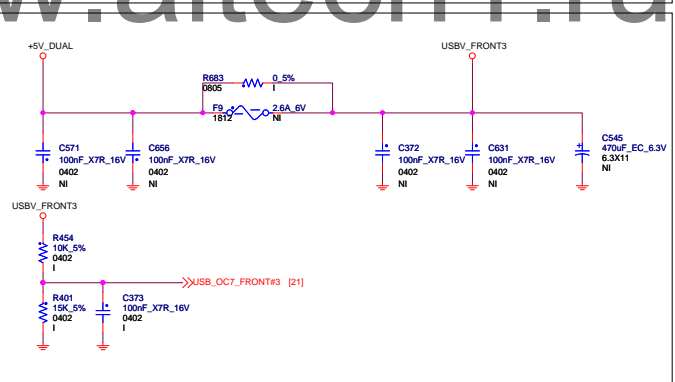
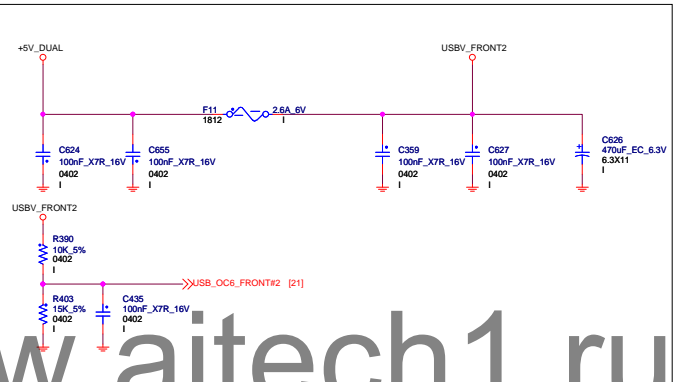
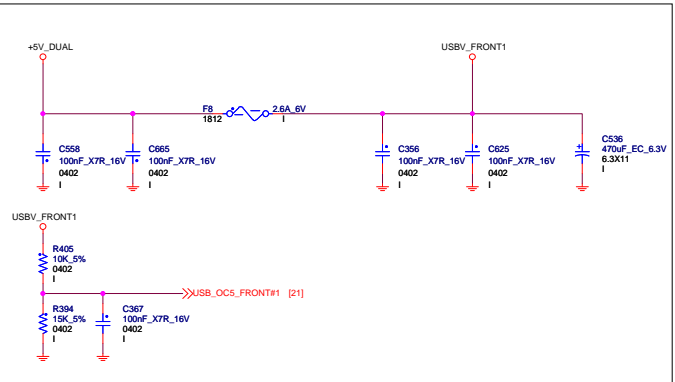
## PCH - CLOCK DISTRIBUTION





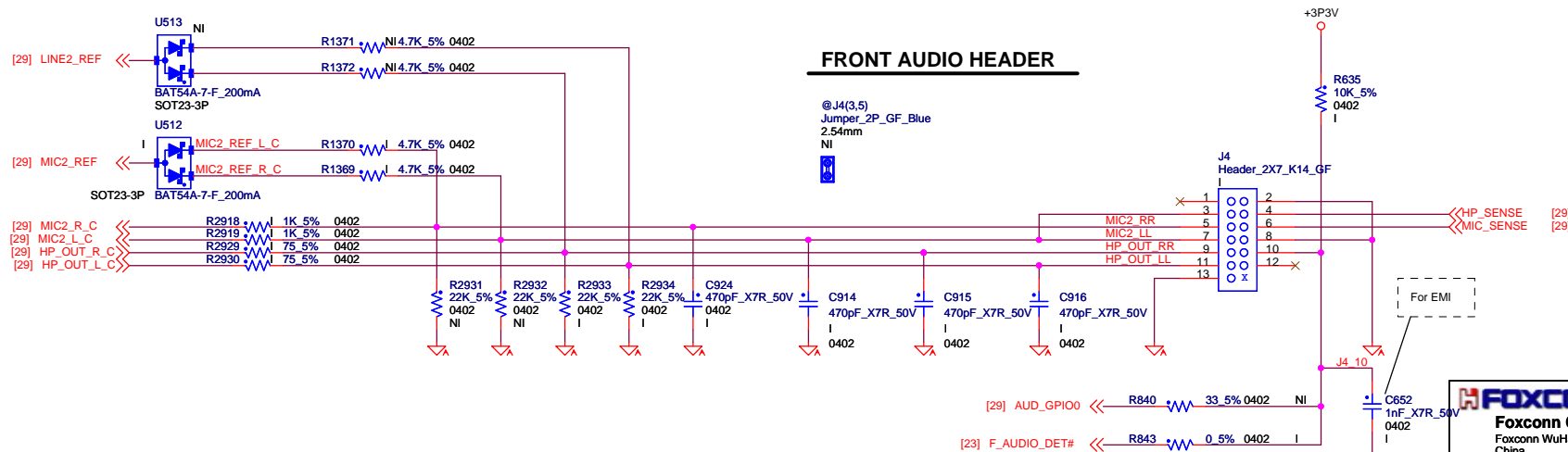
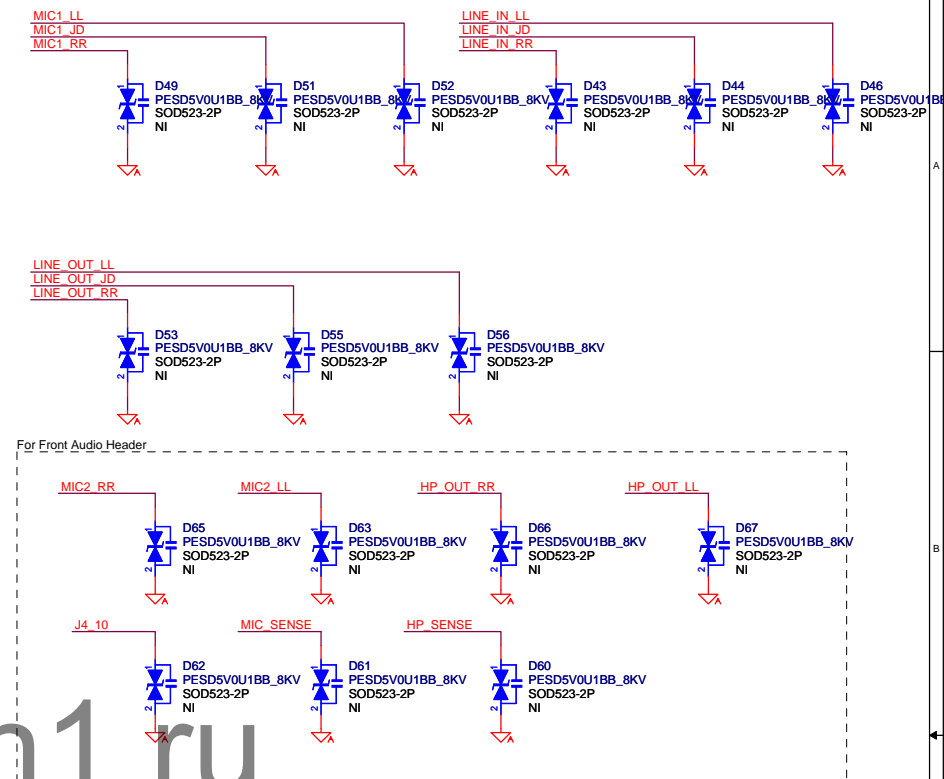
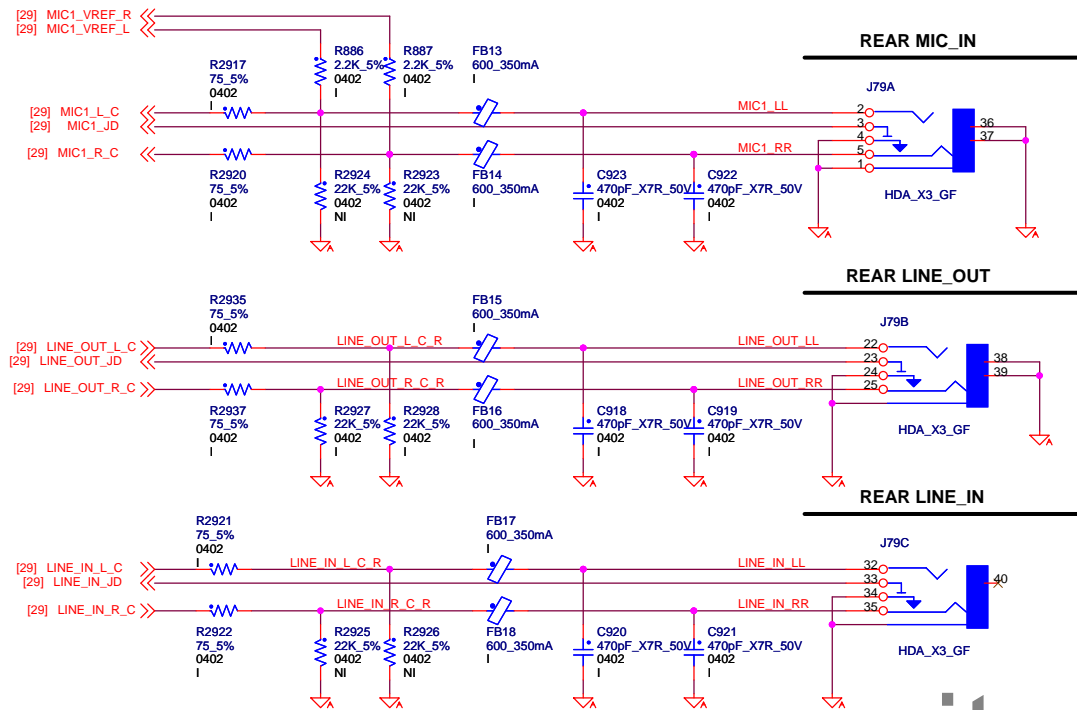


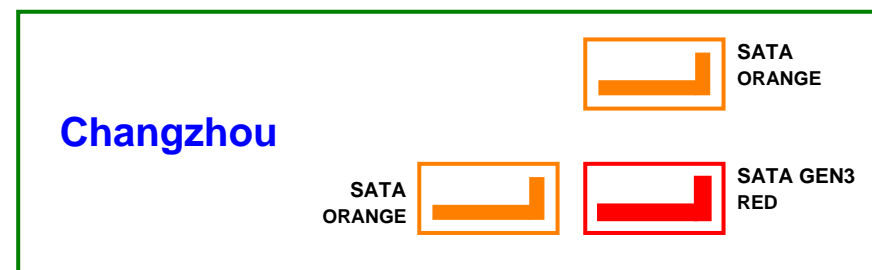
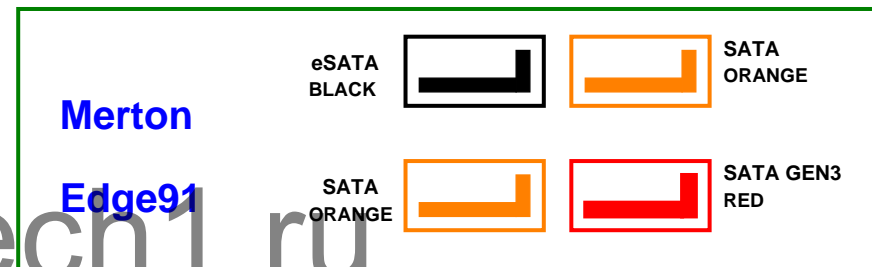
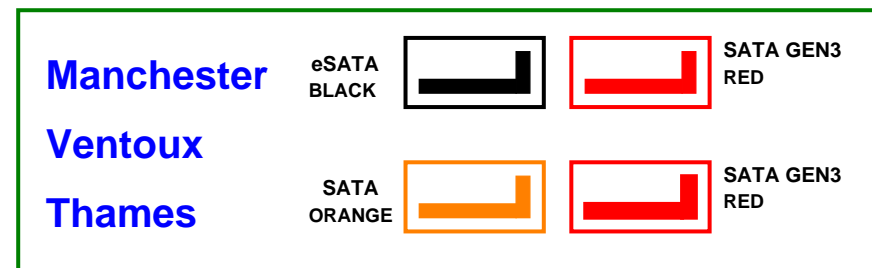
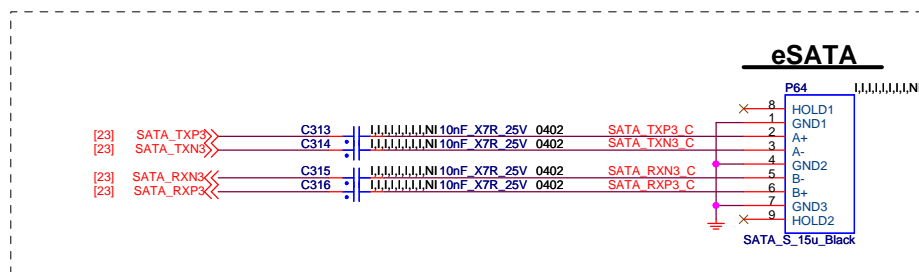
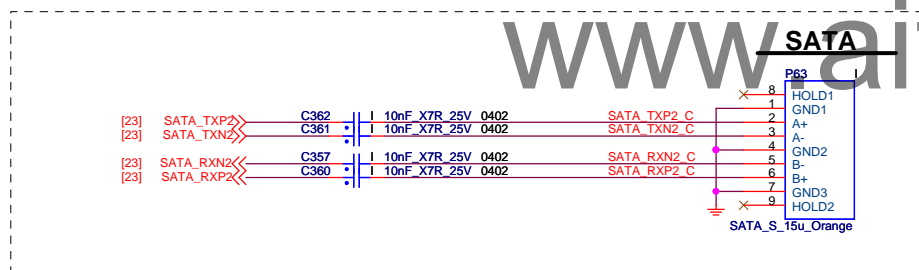
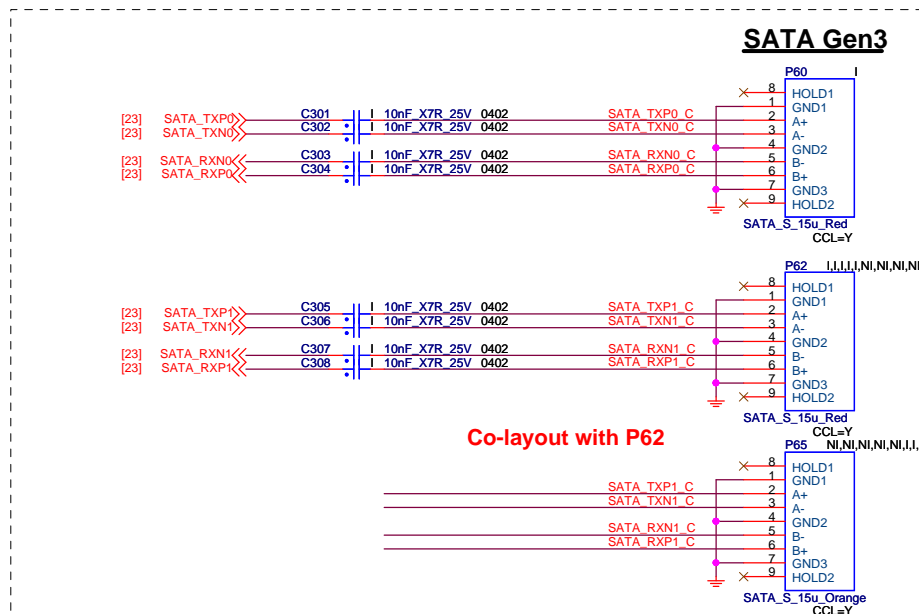




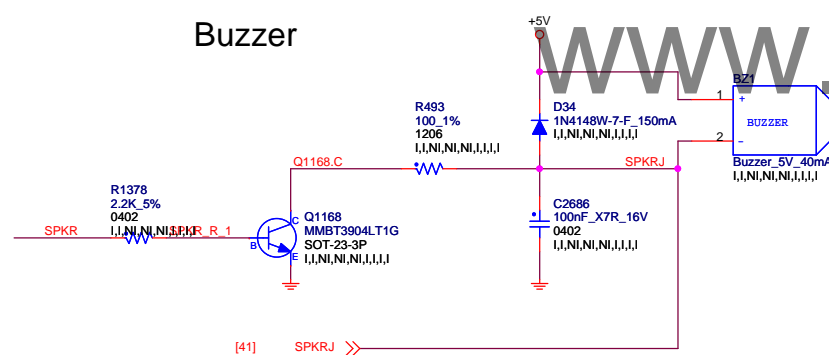
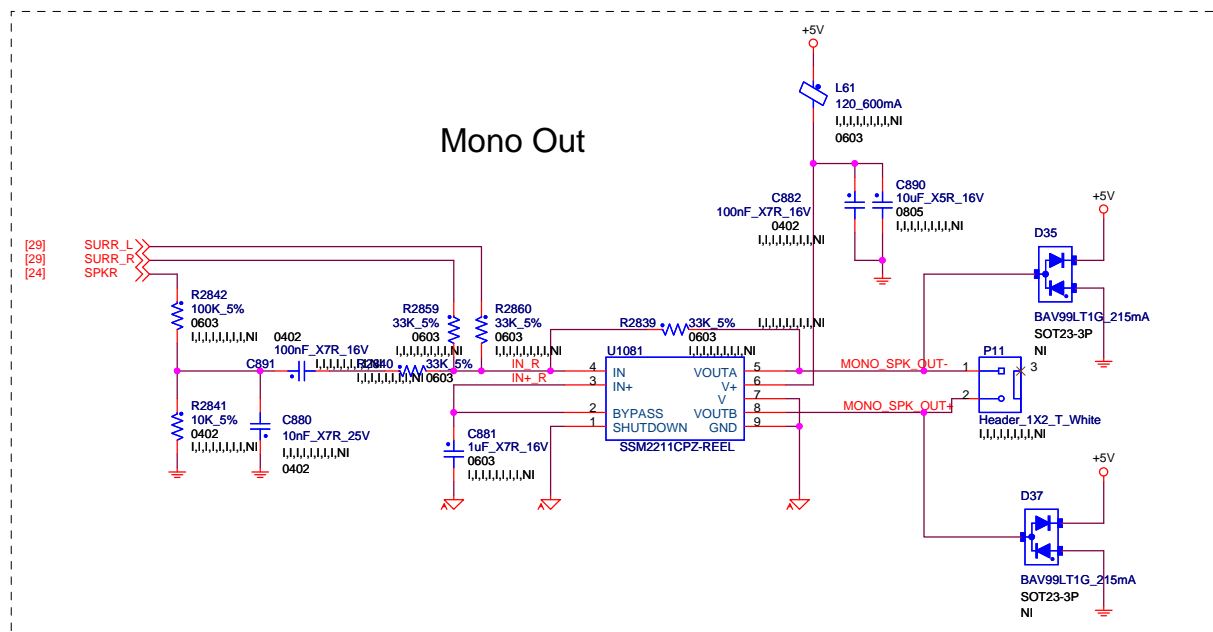




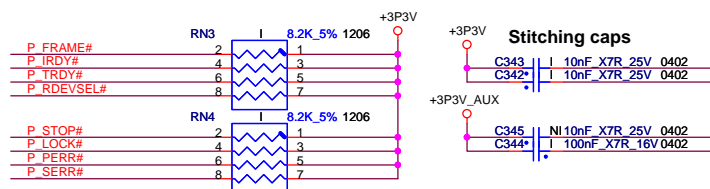
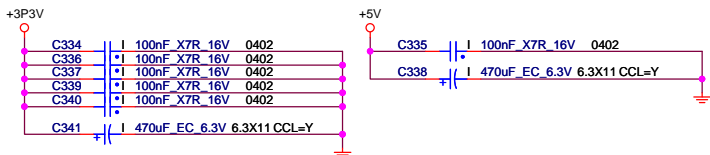
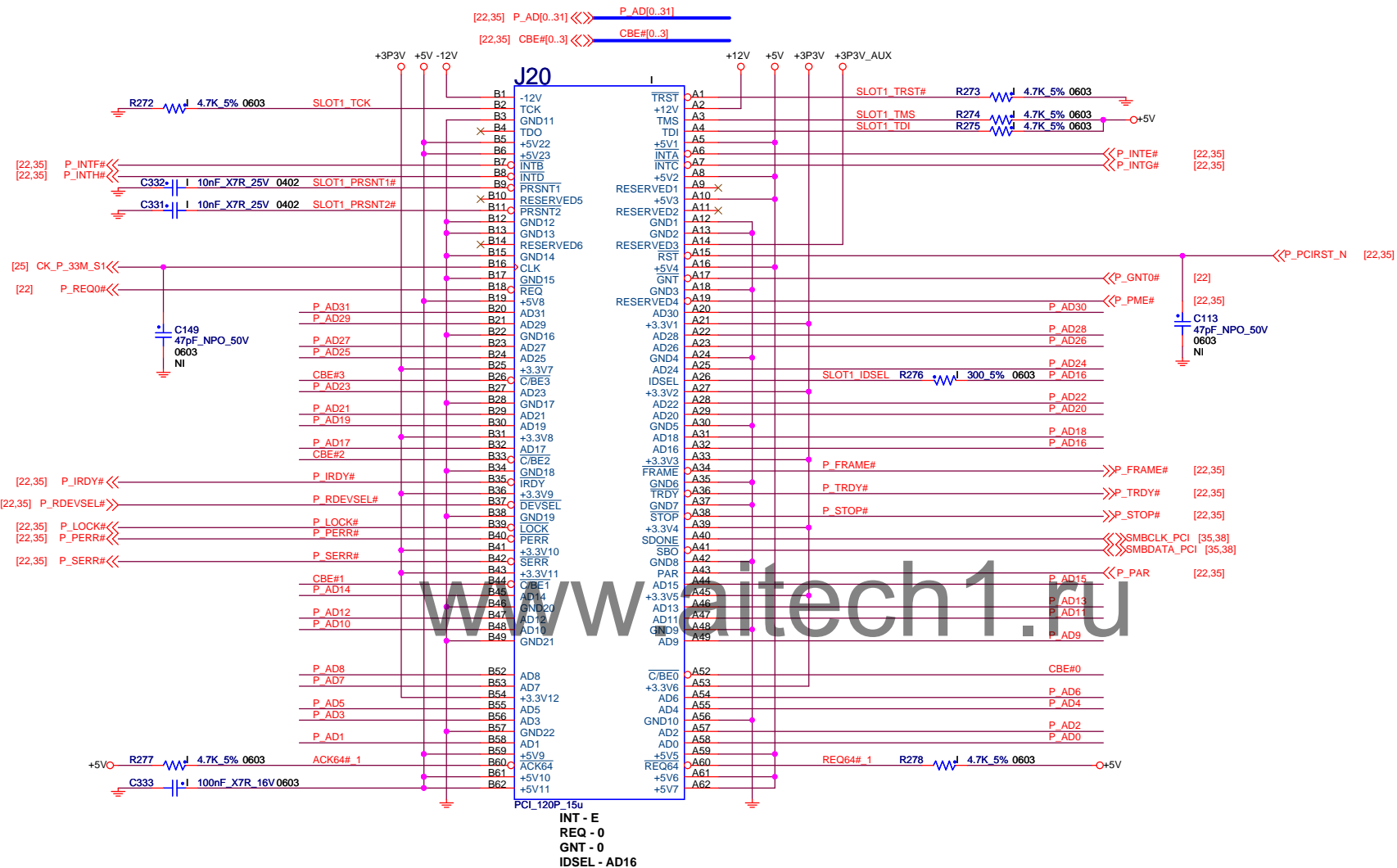




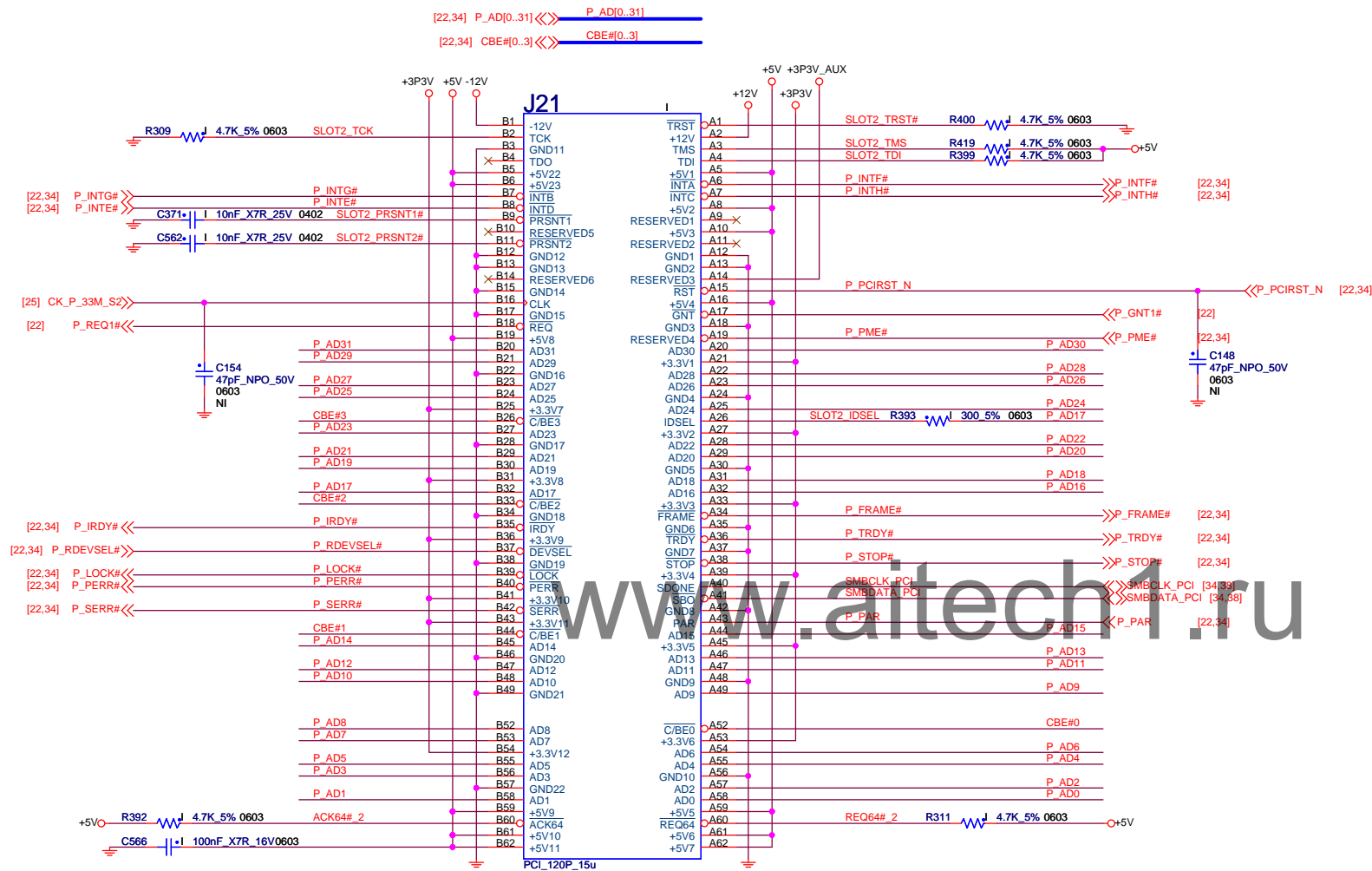




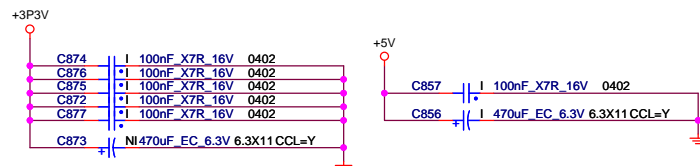
# PCI SLOT 1



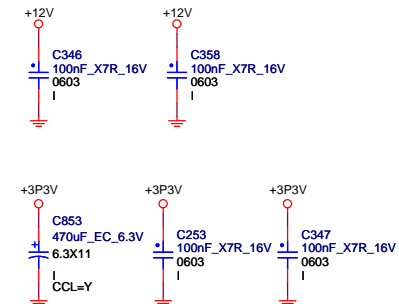
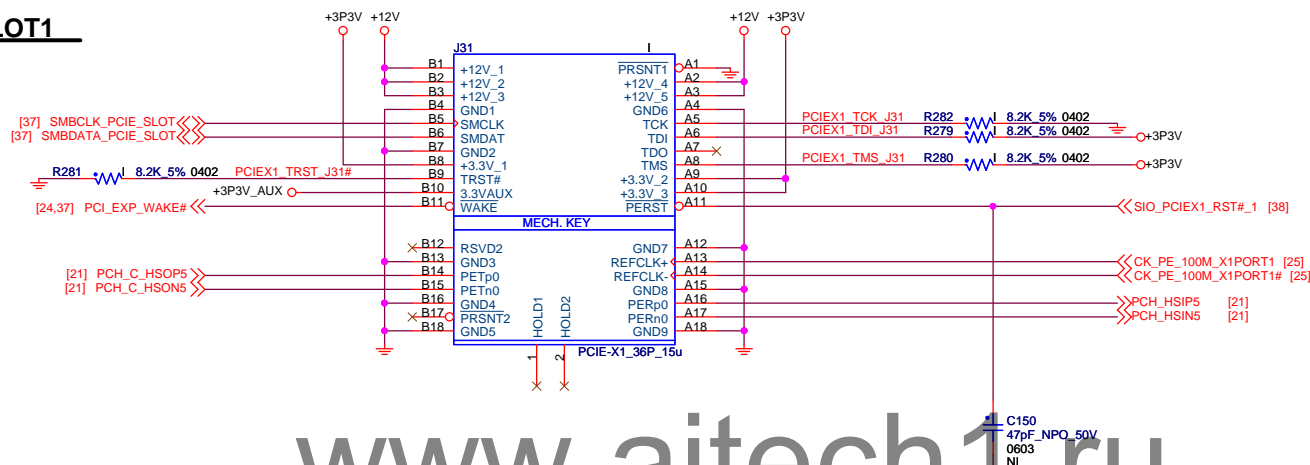
# PCI SLOT



INT - F  
REQ - 1  
GNT - 1  
IDSEL - AD17

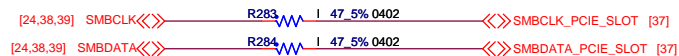


## PCI EXPRESS X1 SLOT1



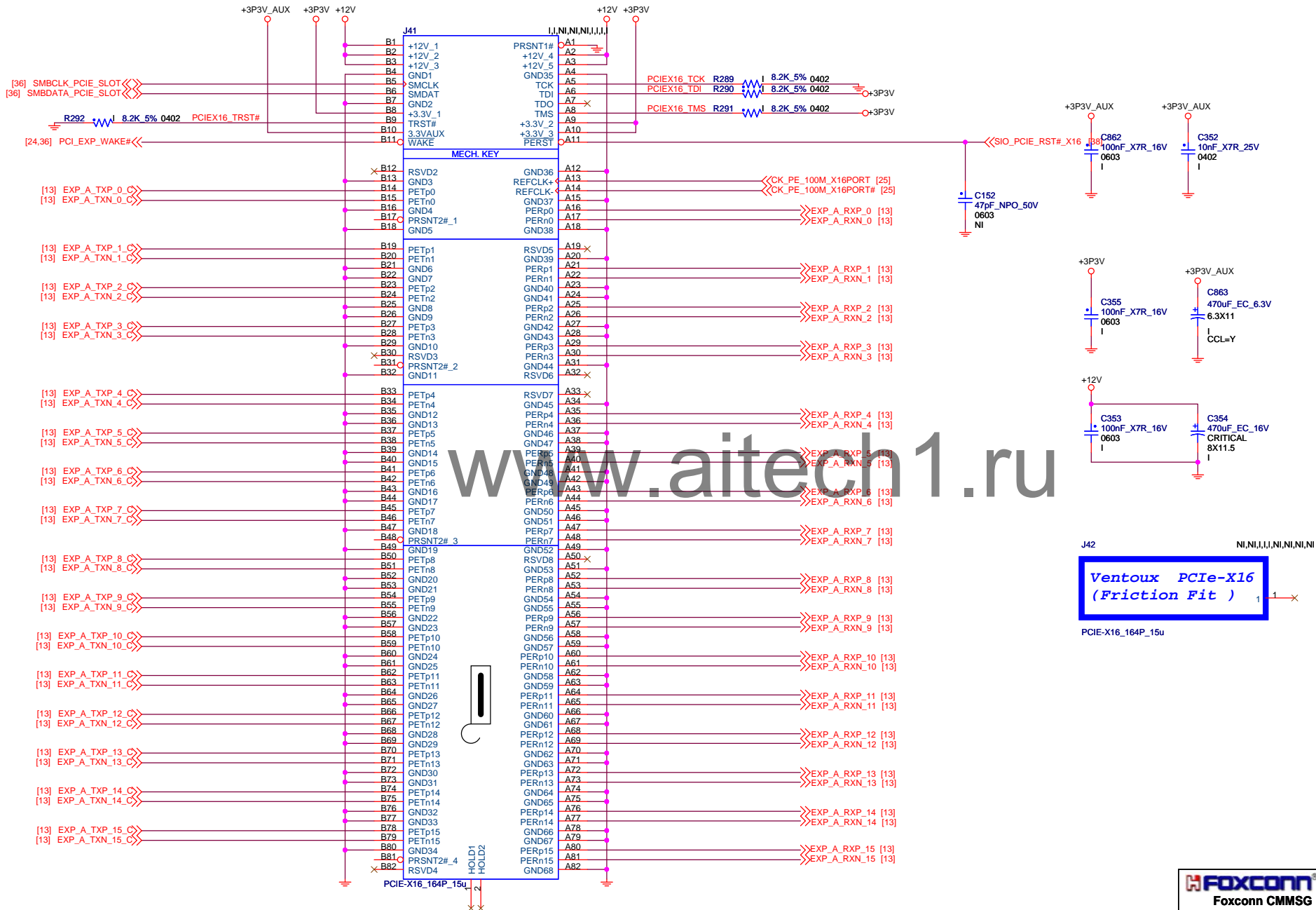
www.aitech1.ru

For Monotonic improve use



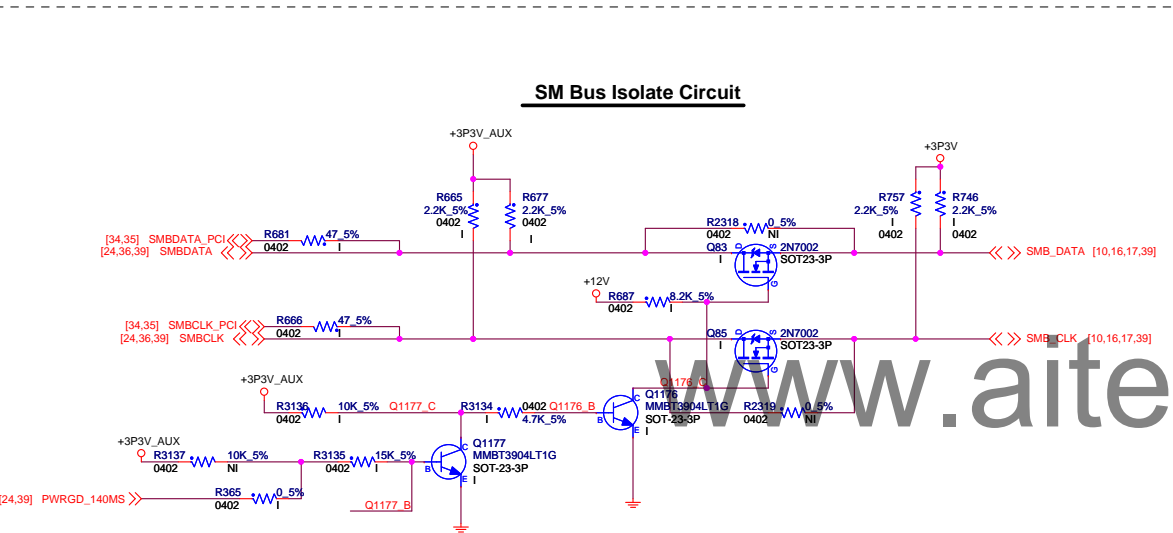
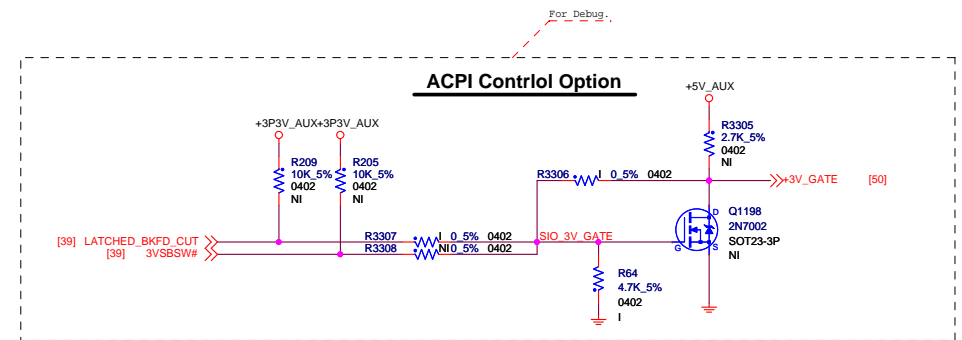
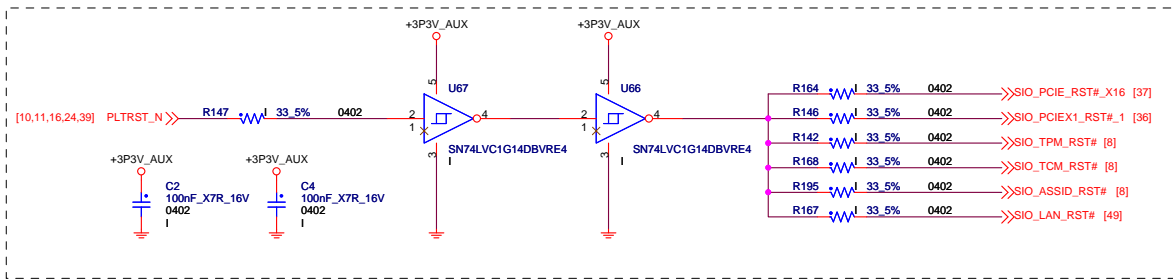


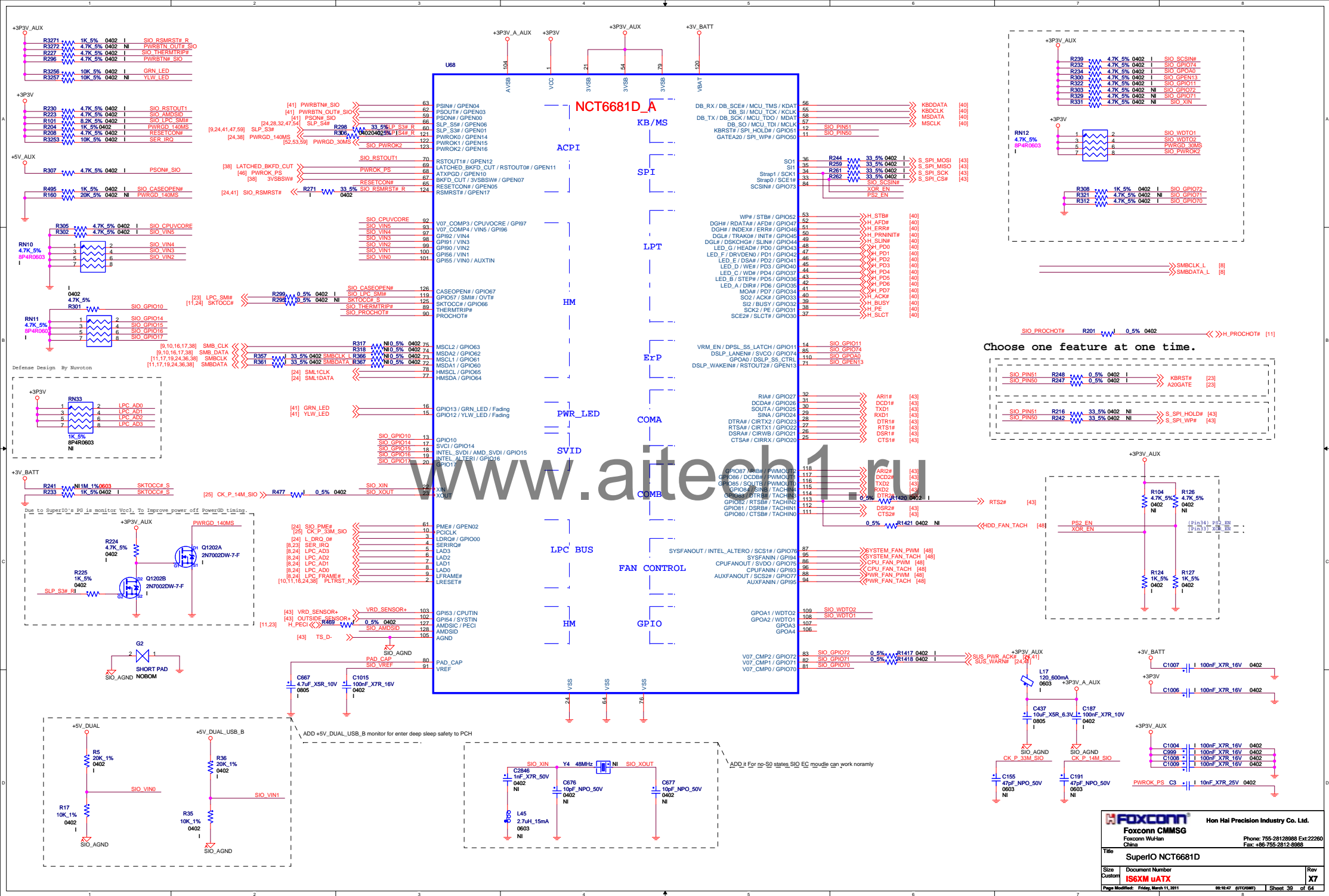
# PCI EXPRESS x16 SLOT



Ventoux PCIe-X16  
(Friction Fit)

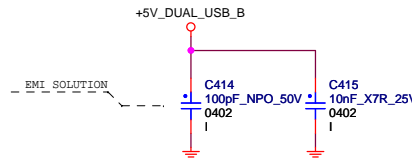
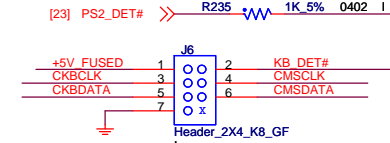
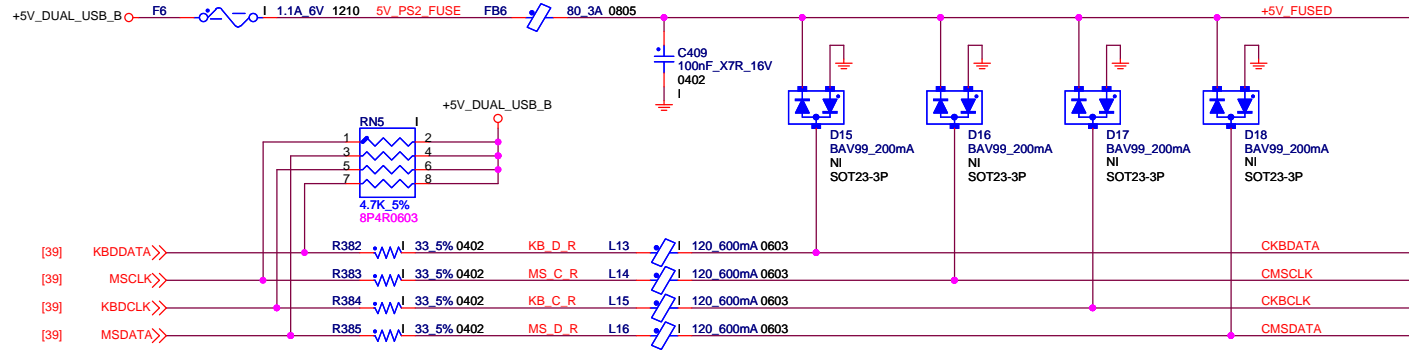
PCIEX16\_164P\_15u



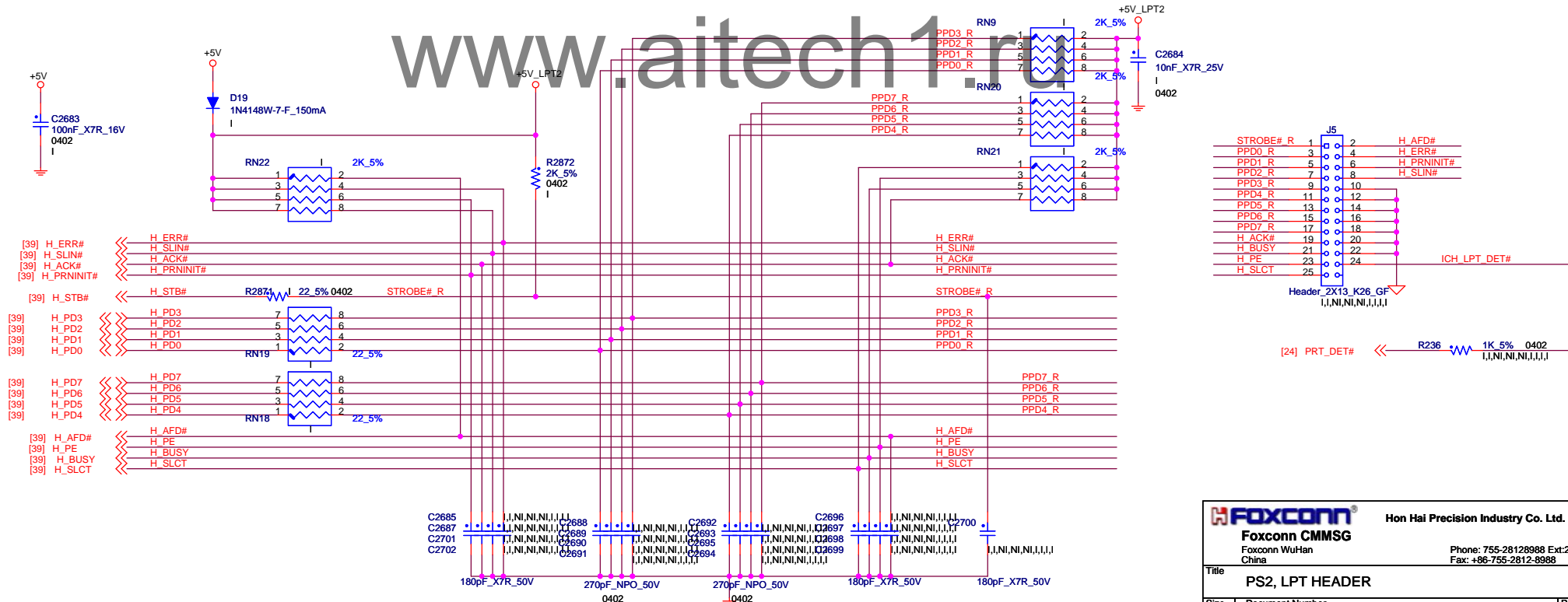
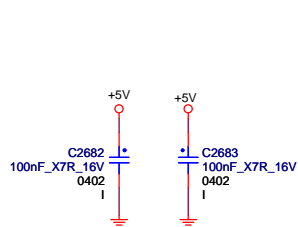


# KEYBOARD / MOUSE

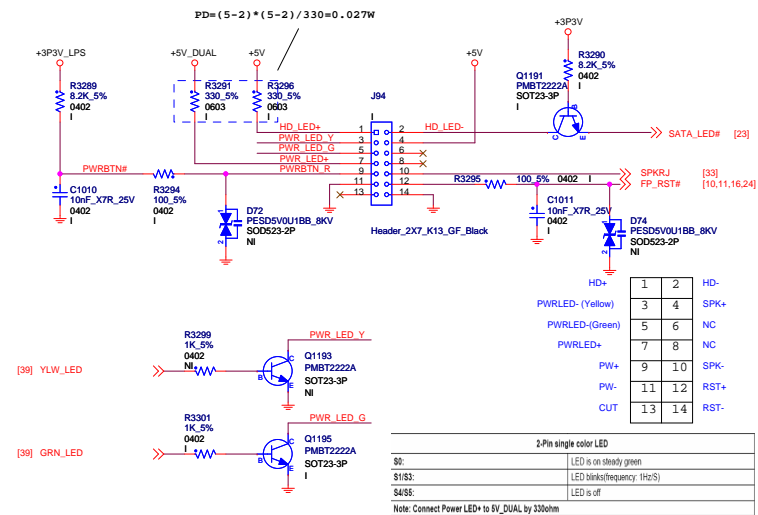
The +5V\_FUSED power trace width must be 40 mils or greater



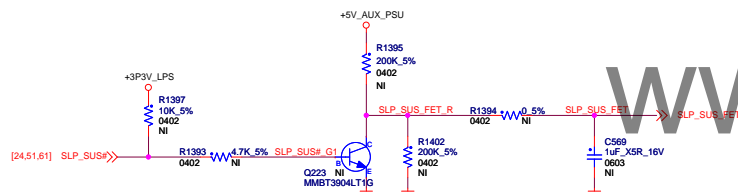
CKBCLK	C410	150pF_NPO_50V	0402
CKBCLK	C411	150pF_NPO_50V	0402
CKBCLK	C412	150pF_NPO_50V	0402
CKBCLK	C413	150pF_NPO_50V	0402



## FRONT PANEL



### DSW CONTROL SIGNAL

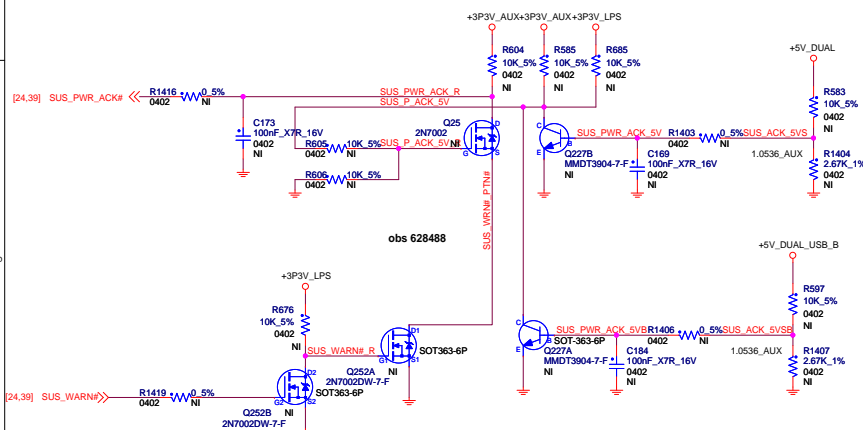


## +5V DUAL SUS ACK

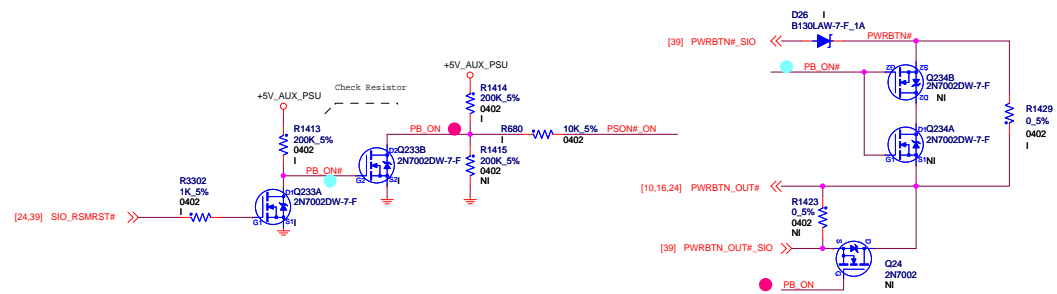
For board bring up, and to insure that the handshake circuit does not prevent the circuit from going into DeepSleep, do the following:  
\* Install R535 \* NI R1405

obs 615987

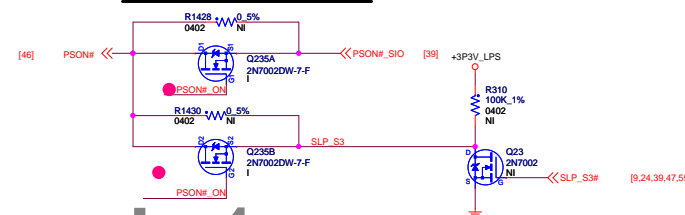
obs 628488



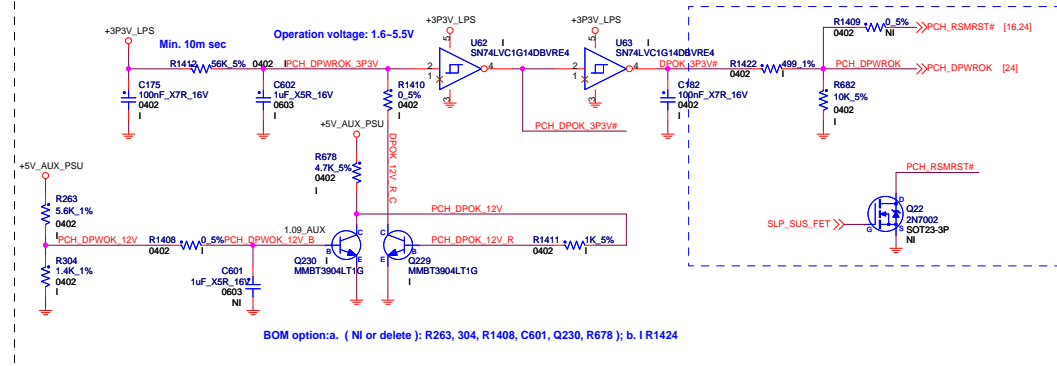
### PowerButton CONTROL LOGIC



### PS\_ON# CONTROL LOGIC



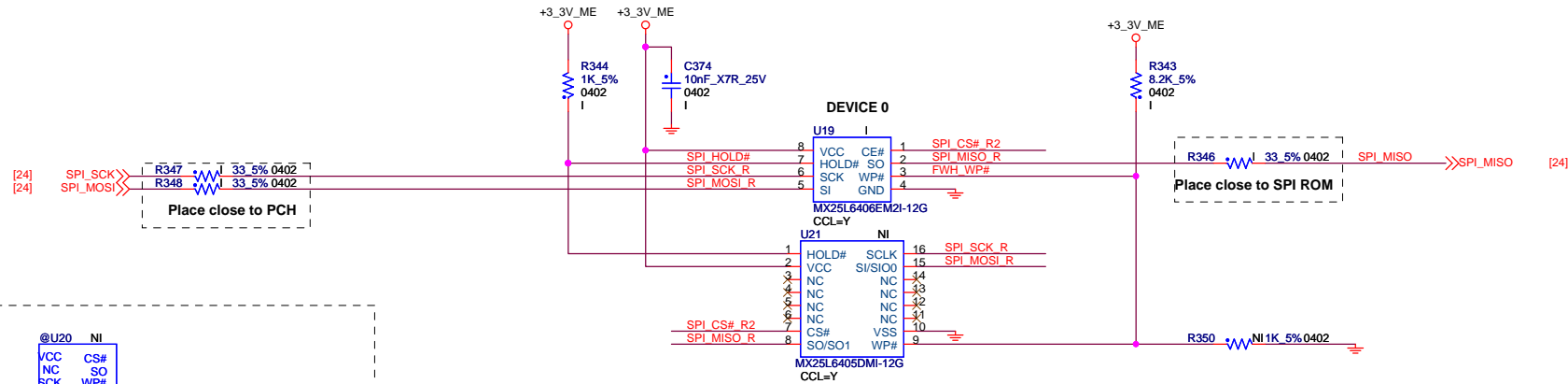
**PCH\_DPWROK**



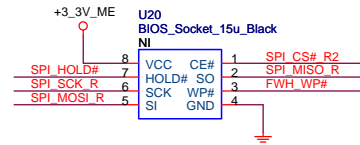
**BOM option:**a. ( NI or delete ): R263, 304, R1408, C601, Q230, R678 ); b. I R1424

## SPI ROM

8 PIN AND 16 PIN SHOULD BE DUAL FOOTPRINT

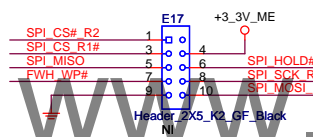


@U20 NI  
VCC CS#  
NC SO  
SCK WP#  
SI GND  
MX25L6406EM2I-12G  
CRITICAL  
DIP  
PN same with U19, only for BOM on sample phase.



Add socket for Sample phase debug

## SPI ROM Debug Header



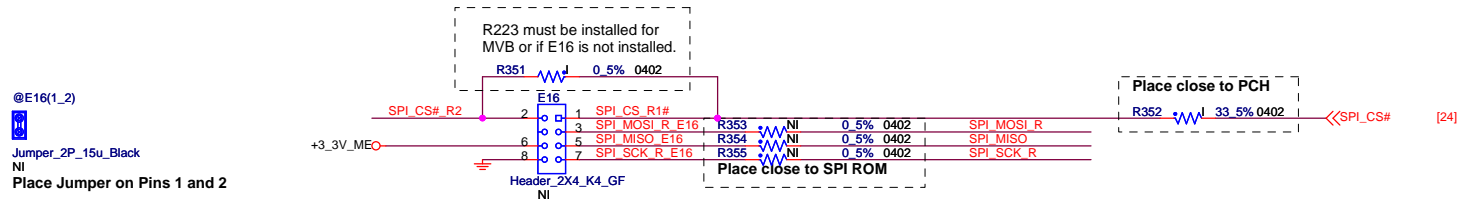
@E17(1,3)  
Jumper\_2P\_GF\_Black  
NI

SPI DEBUG: Header color: -  
pin1: SPI\_CS#(to SB) pin2: CUT  
pin3: SPI\_CS#(to SB) pin4: +VSP  
pin5: SPI\_MISO\_R pin6: SPI\_HOLD#  
pin7: SPI\_WP# pin8: SPI\_SCK\_R  
pin9: GND pin10: SPI\_MOSI\_R

Header and Jumper datasheet as attached file:

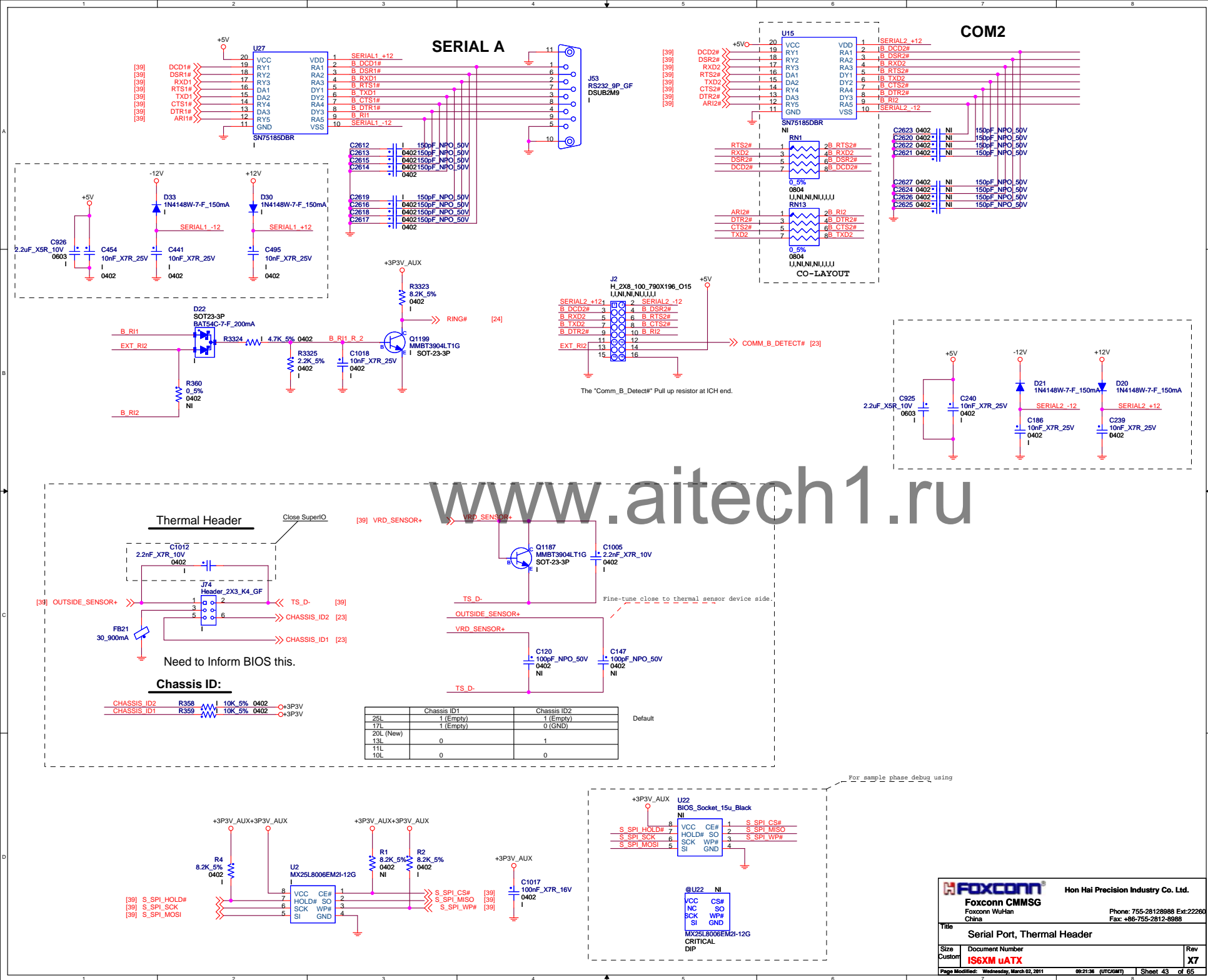
## SPI ROM BOOTBLOCK HEADER/JUMPER

The header traces should be daisy-chain through the header with no stubs.



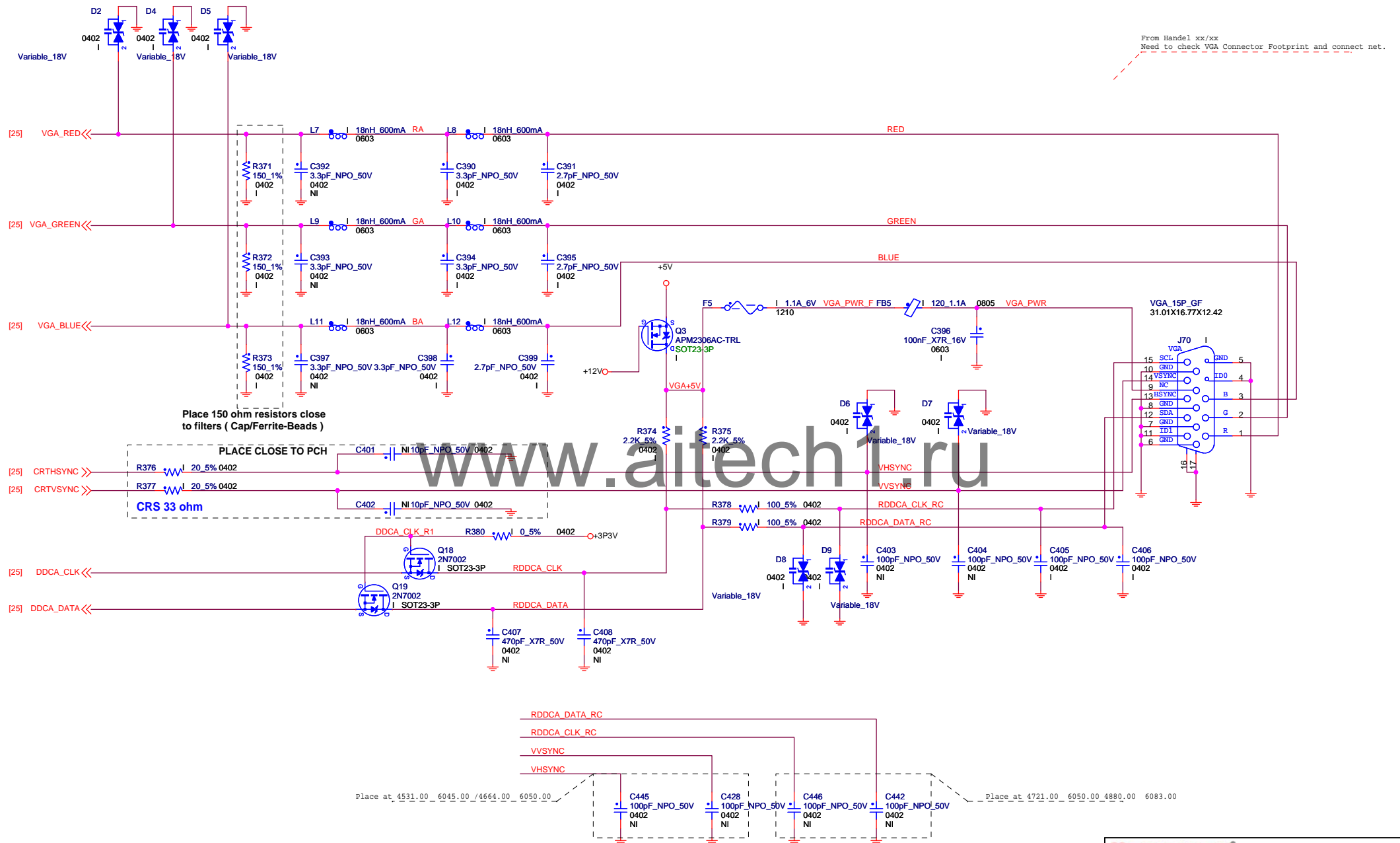
@E16(1,2)  
Jumper\_2P\_15u\_Black  
NI  
Place Jumper on Pins 1 and 2



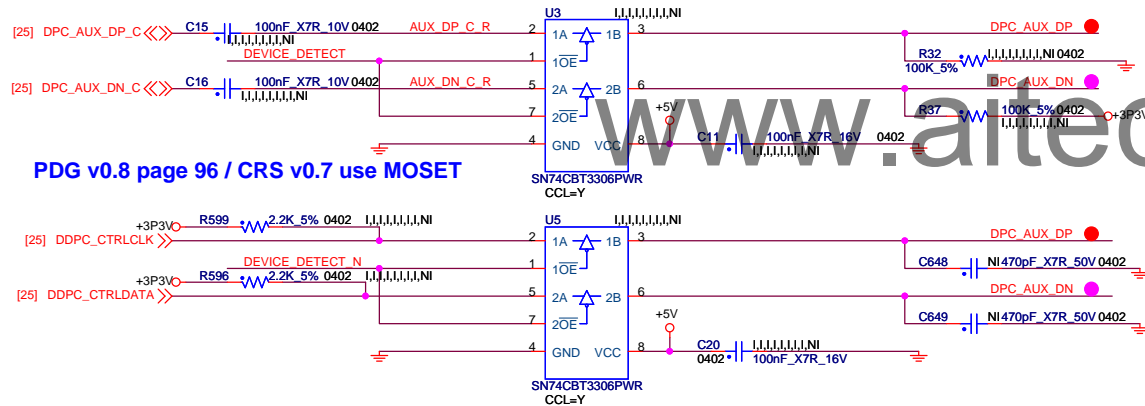
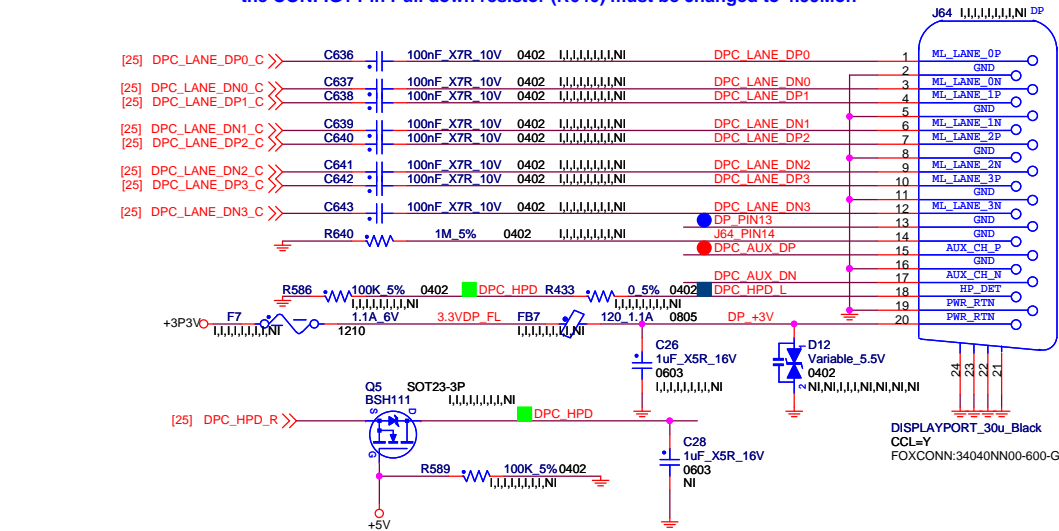


www.aitech1.ru

# RGB ESD PROTECTION

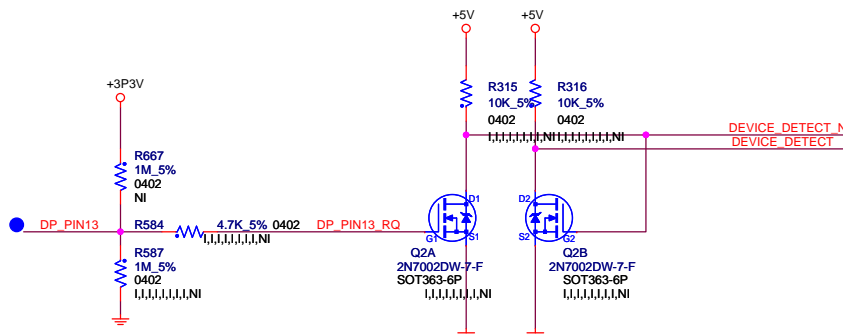


If the Upstream device is a dual-mode device and supports HDMI, then the CONFIG1 Pin Pull down resistor (R640) must be changed to 4.99Moh

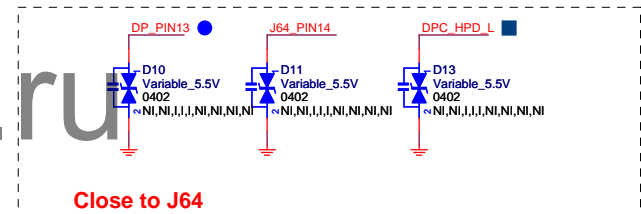
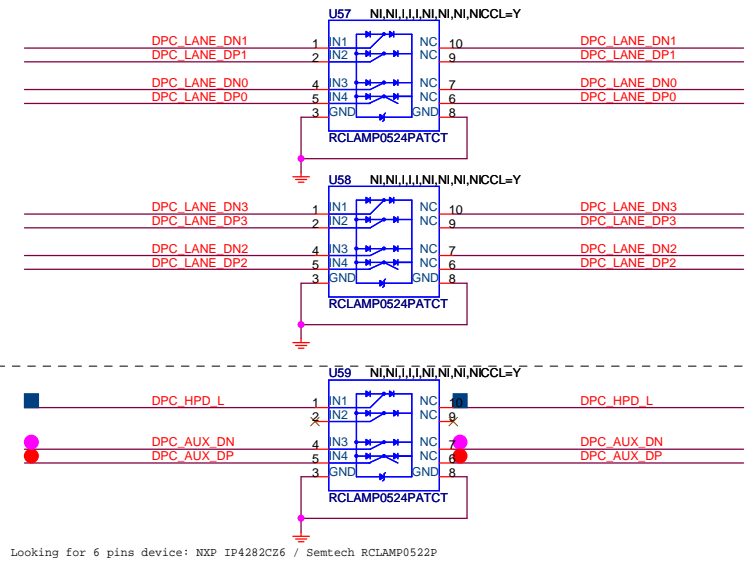


PDG v0.8 page 96 / CRS v0.7 use MOSET

PIN13		FUNCTION
DP	DONGLE	
L	X	DEVICE_DETECT
X	H	DEVICE_DETECT_N

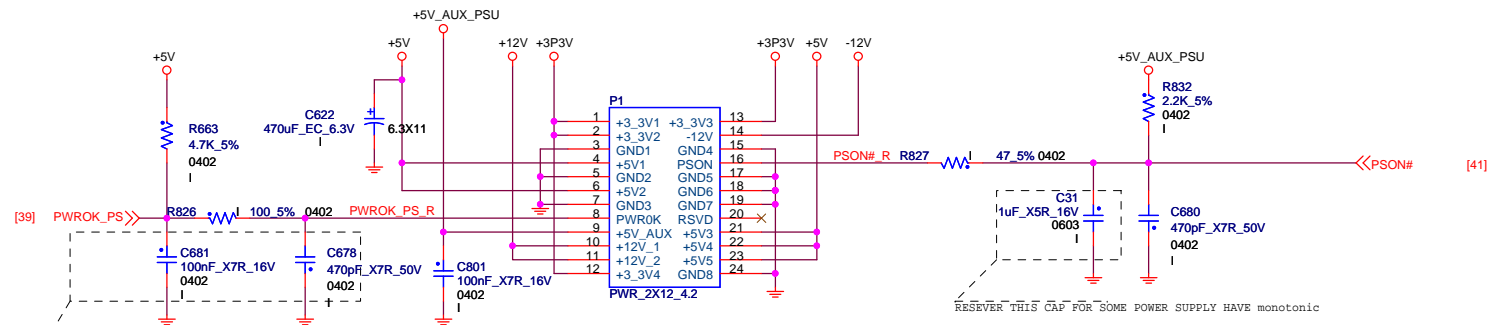


## ESD suppressor



Close to J64

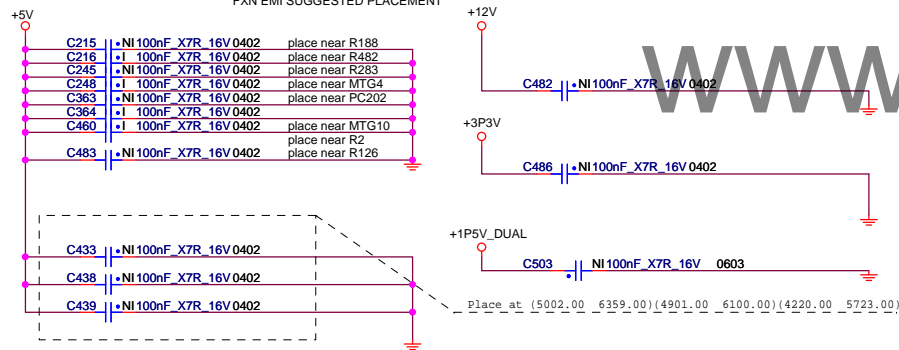
## Power Input Connector



Add these cap for some power supply have noise

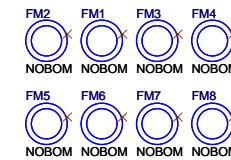
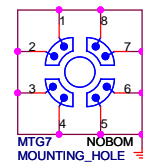
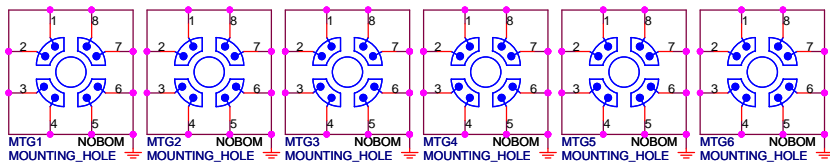
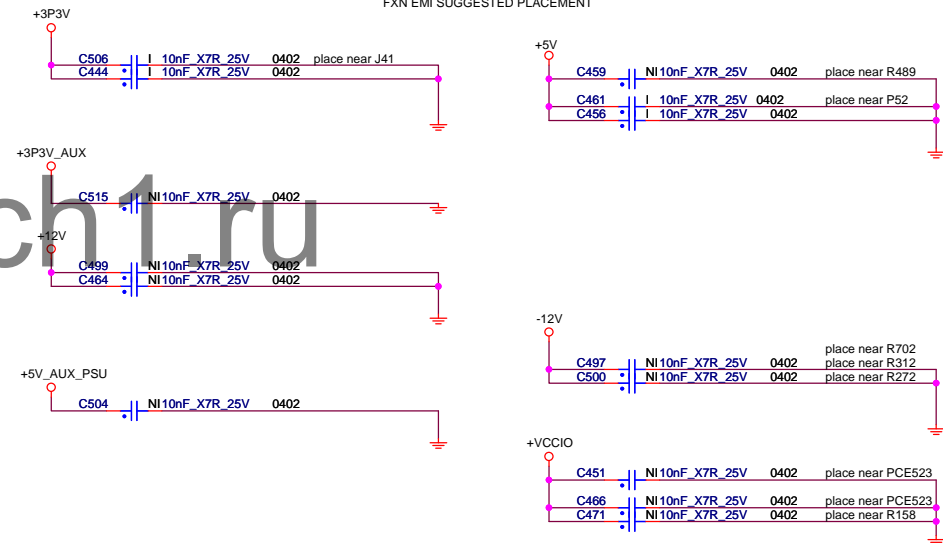
## EMI CAP

FXN EMI SUGGESTED PLACEMENT

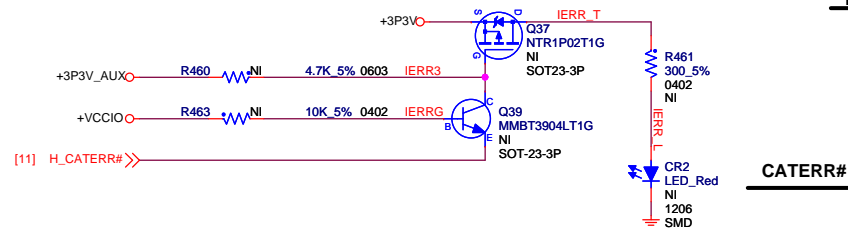


## EMI CAP

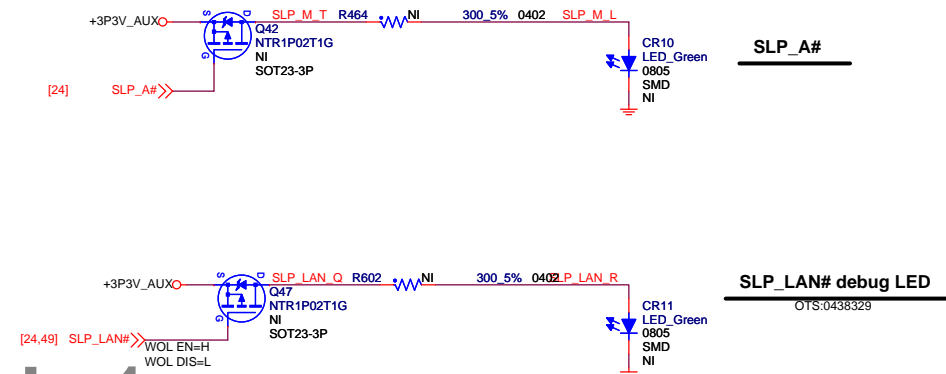
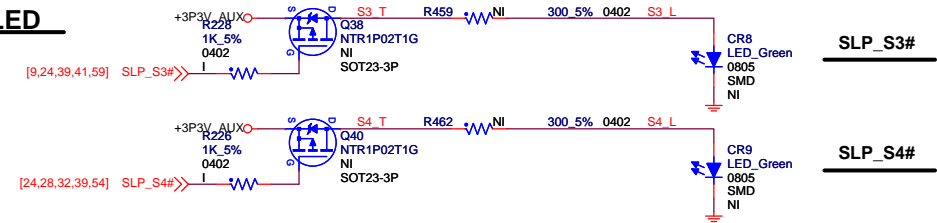
FXN EMI SUGGESTED PLACEMENT



<b>FOXCONN</b> <b>Foxconn CMMSG</b> Foxconn Wuhan China		<b>Hon Hai Precision Industry Co. Ltd.</b> Phone: 755-28128988 Ext:22260 Fax: +86-755-2812-8988	
<b>POWER INPUT / EMI CAP</b>			
Title Size Custor	Document Number <b>IS6XM uATX</b>		Rev <b>X7</b>
Page Modified: Wednesday, March 02, 2011 09:21:37 (UTC+08:00) Sheet 46 of 65			

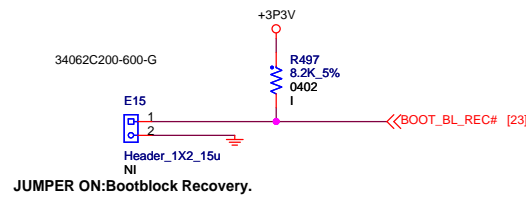


## PCA LED

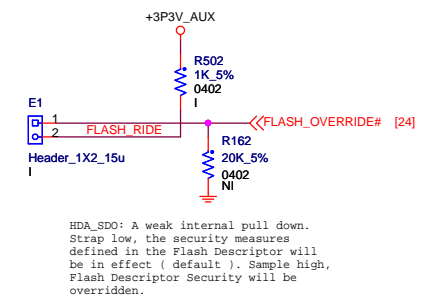


## BOOTBLOCK RECOVERY

E15: SPI ROM bootblock recovery header

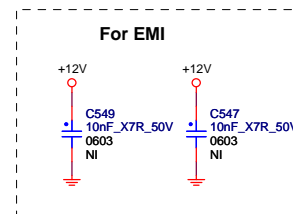
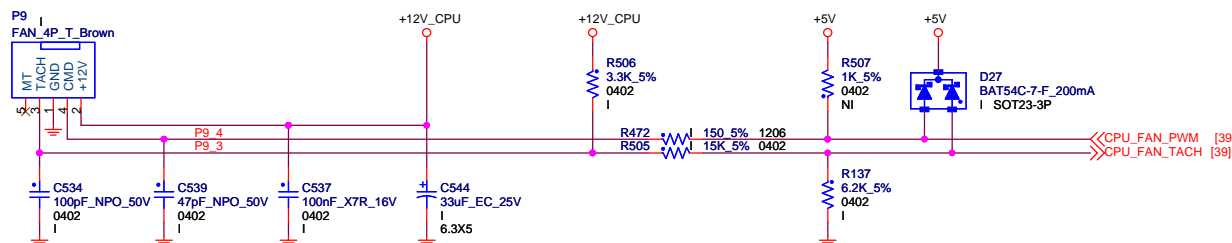


## FLASH OVERRIDE



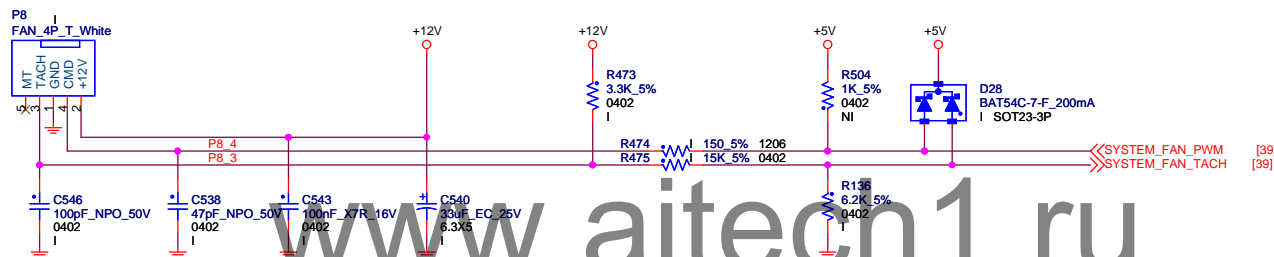
## CPU FAN

Color: Brown



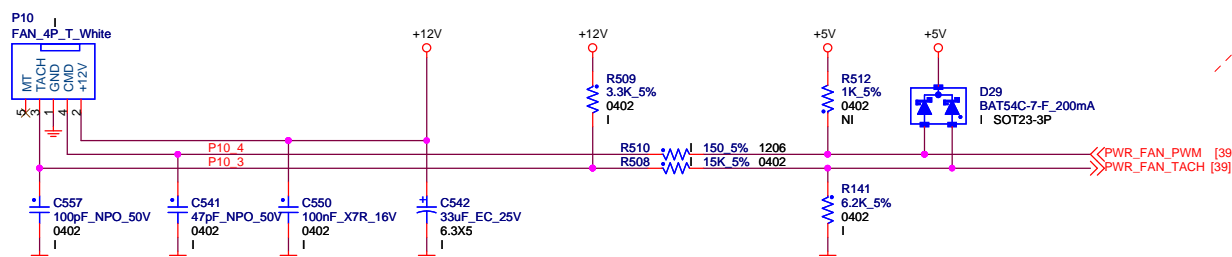
## SYSTEM FAN

Color: White



## PWR FAN

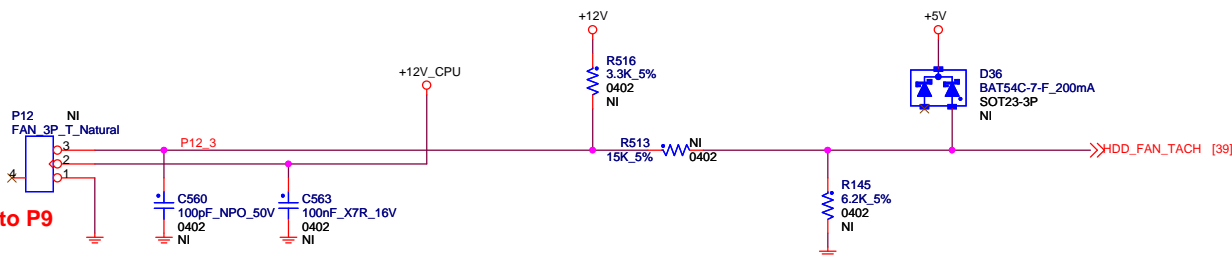
Color: White



From Kansas  
- Check PWR FAN color  
- Follow thermal spec add +5v pull up (Reserved)

## HDD FAN

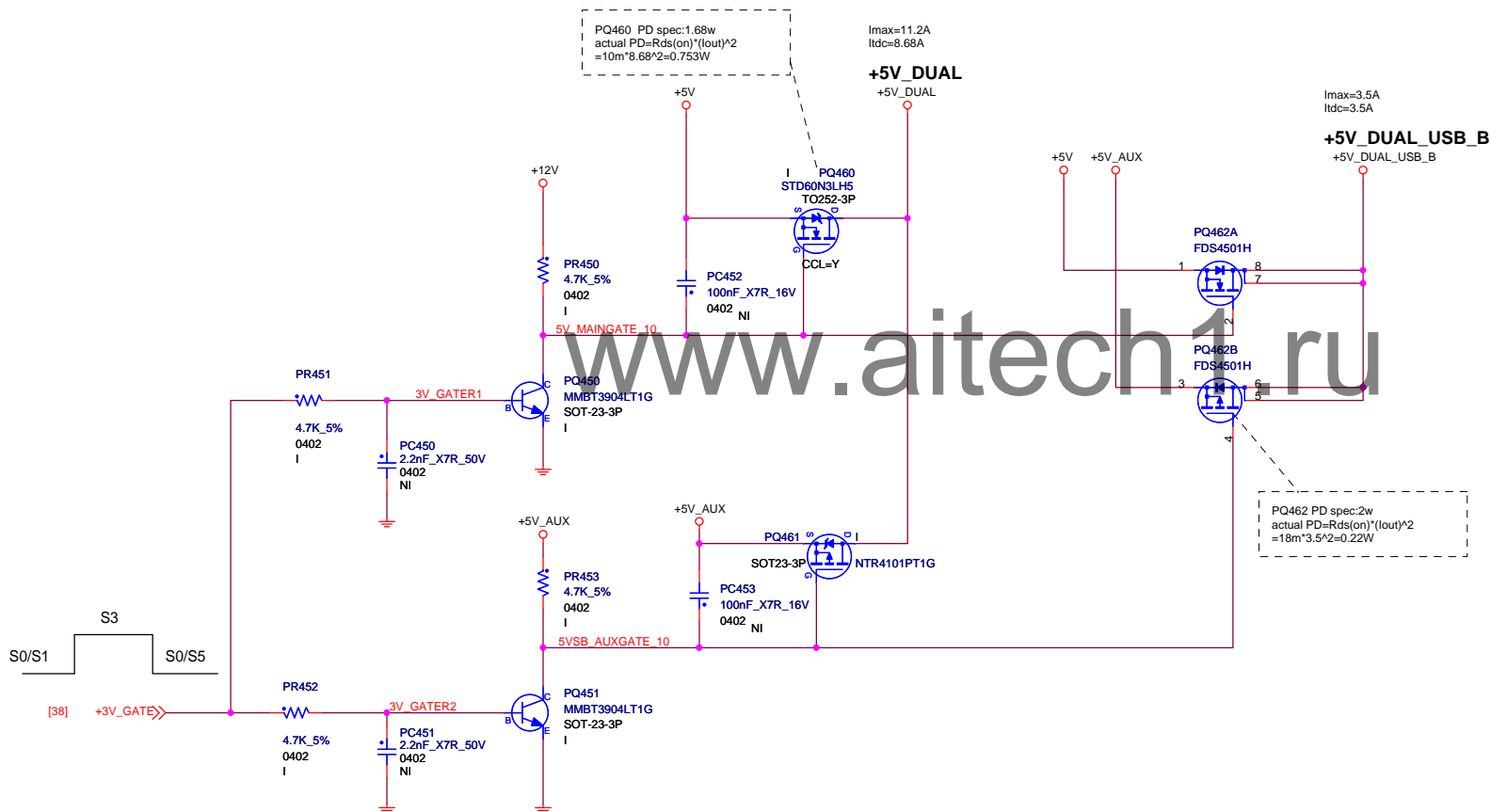
Color: White



P12 Close to P9




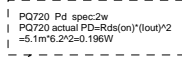
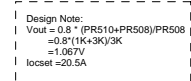


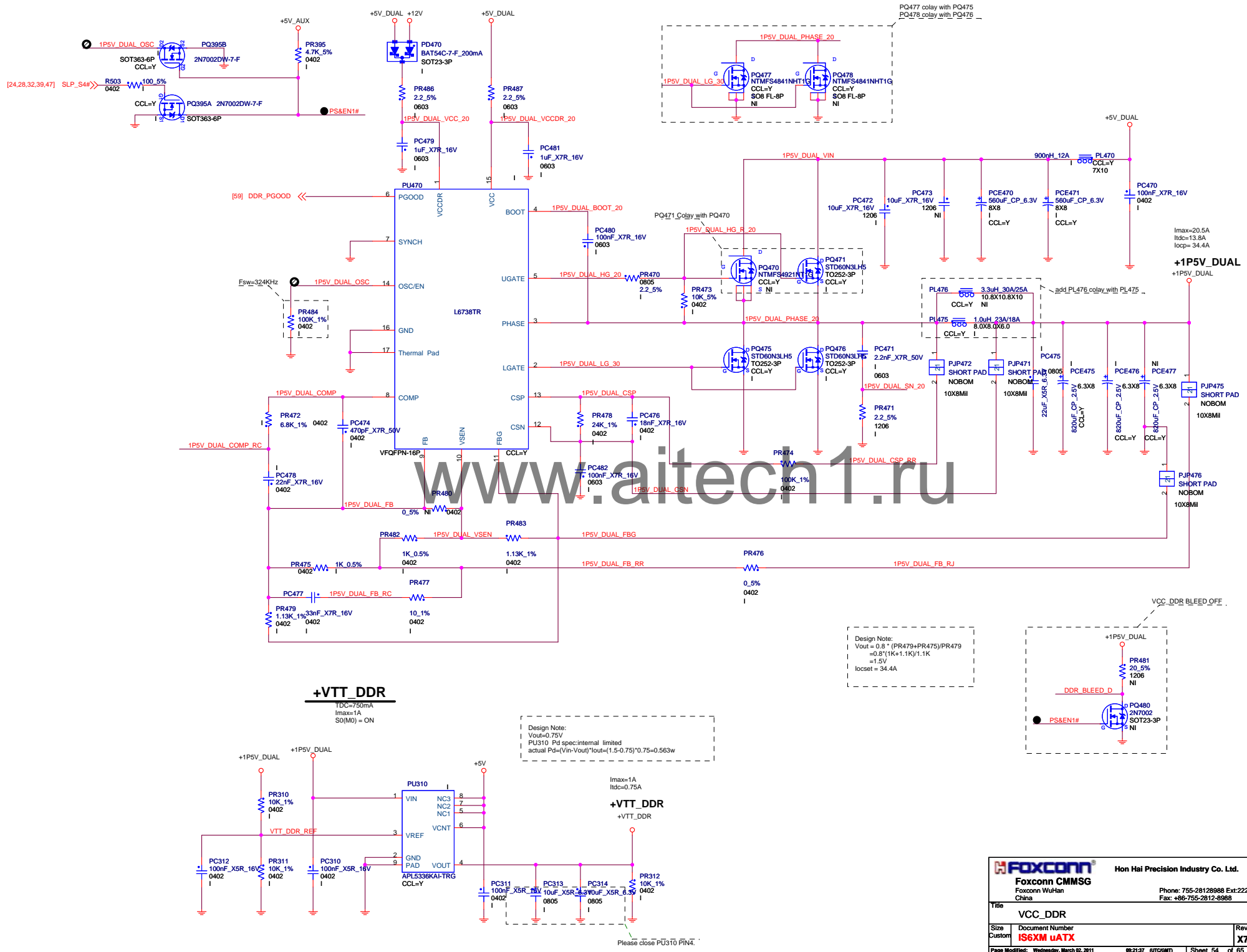




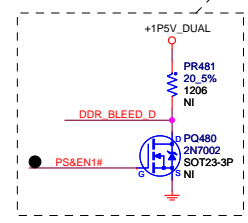


		Hon Hai Precision Industry Co. Ltd.	
<b>Foxconn CMMSG</b> Foxconn Wuhan China		Phone: 755-28128988 Ext:2229 Fax: +86-755-2812-8988	
<b>Title</b> +1P8V_SFR			
<b>Size Custom</b> Document Number <b>IS6XM uATX</b>		<b>Rev</b> <b>X7</b>	
<b>Page Modified:</b> Wednesday, March 02, 2011		09:21:33 (UTC+08T) Sheet 52 of 65	



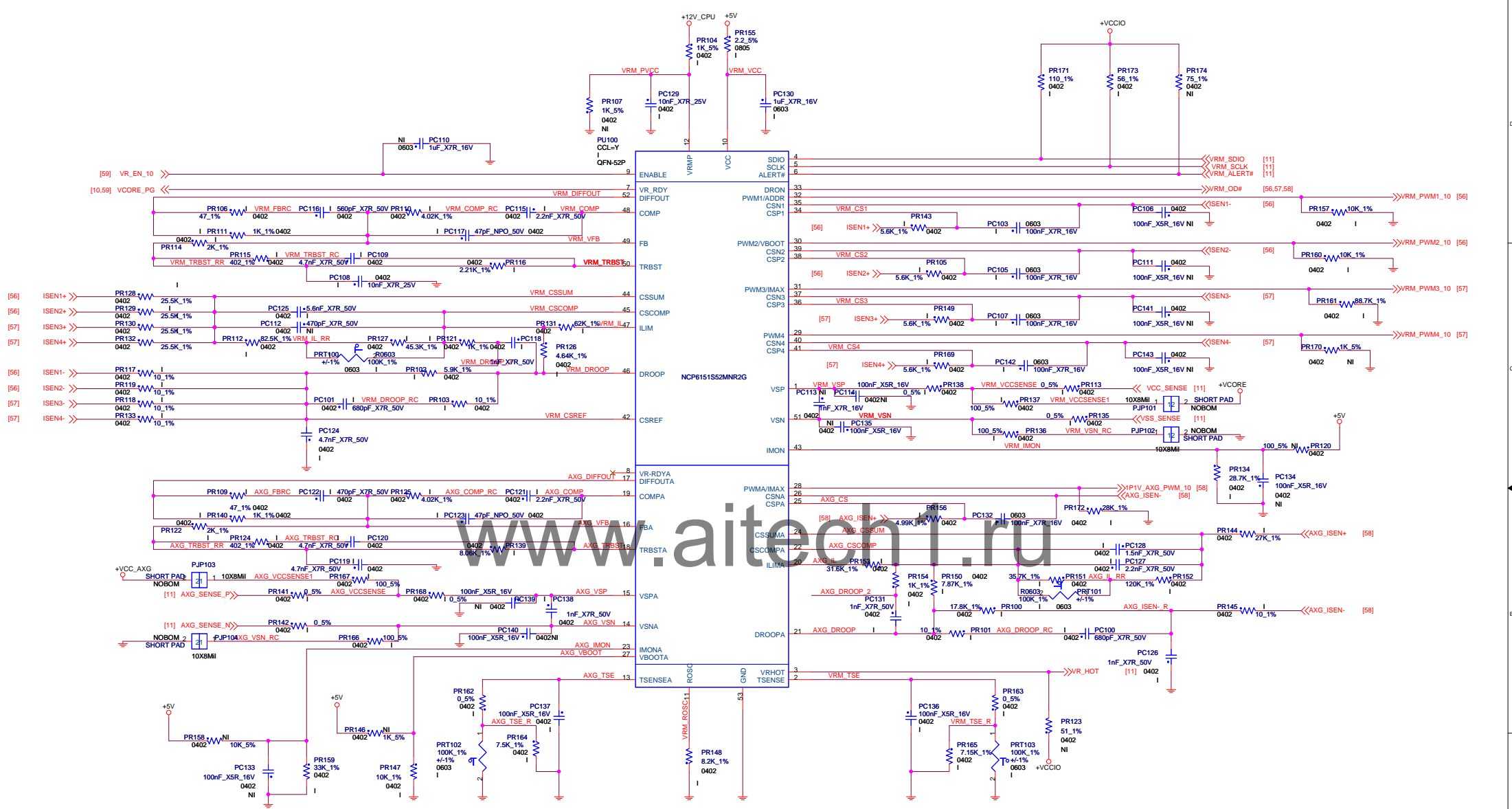


Design Note:  
Vout = 0.8 \* (PR479+PR475)/PR479  
= 0.8\*(1K+1.1K)/1.1K  
= 1.5V  
Iocset = 34.4A



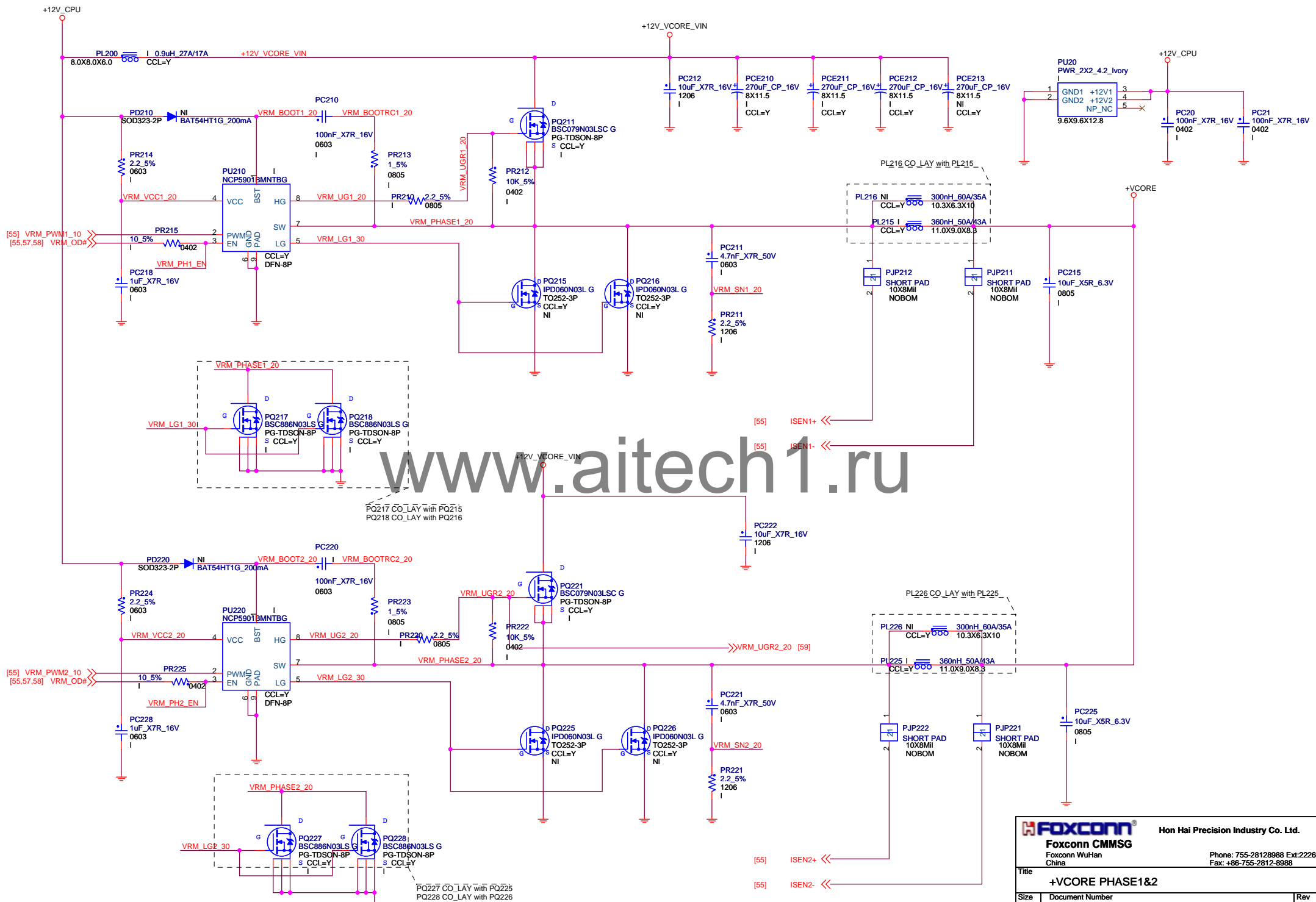
Design Note:  
Vout=0.75V  
PU310: Pd spec internal limited  
actual Pd=(Vin-Vout)\*Iout=(1.5-0.75)\*0.75=0.563w

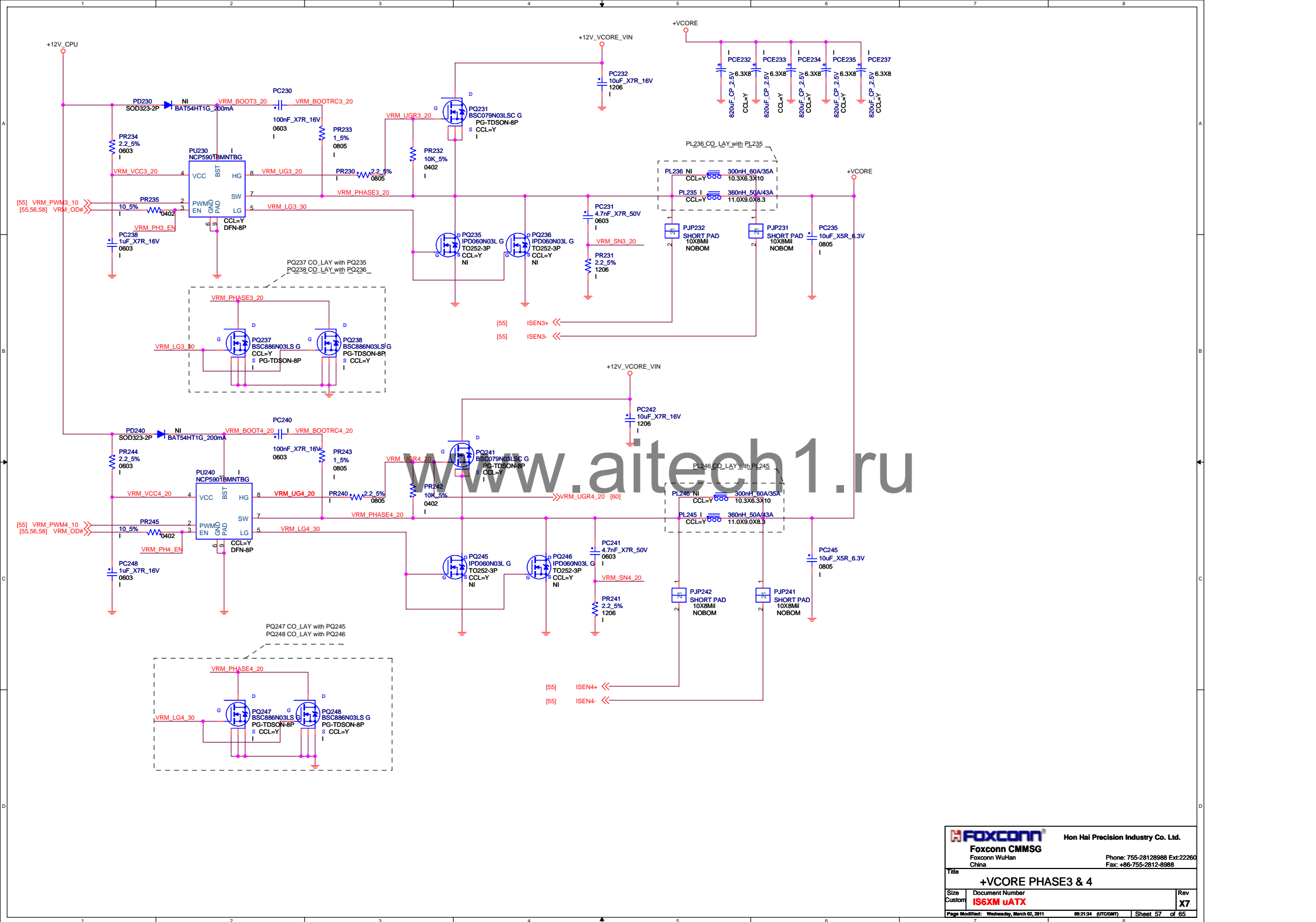




Design Note:  
Vcore OCP :  
 $I_{ocpset} = R_{limit} * 10u * R_{ph} / [R_{cs2} + R_{cs1} * R_{th} / ((R_{cs1} + R_{th}))] / DCR$   
 $R_{cs2} \& PR112 = 82.5K$   
 $R_{cs1} \& PR127 = 35.7K$   
 $R_{th} \& PR100 = 100K$   
 $R_{ph} \& PR128 = 25.5K$   
 $R_{limit} \& PR131 = 62K$   
 $DCR = 0.65mohm$   
 $I_{ocpset} = 223.5A$

Design Note:  
AXG OCP :  
 $I_{ocpset} = R_{limit} * 10u * R_{ph} / [R_{cs2} + R_{cs1} * R_{th} / ((R_{cs1} + R_{th}))] / DCR$   
 $R_{cs2} \& PR152 = 82.5K$   
 $R_{cs1} \& PR151 = 35.7K$   
 $R_{th} \& PR101 = 100K$   
 $R_{ph} \& PR144 = 27K$   
 $R_{limit} \& PR153 = 31.6K$   
 $DCR = 1.05mohm$   
 $I_{ocpset} = 74.6A$



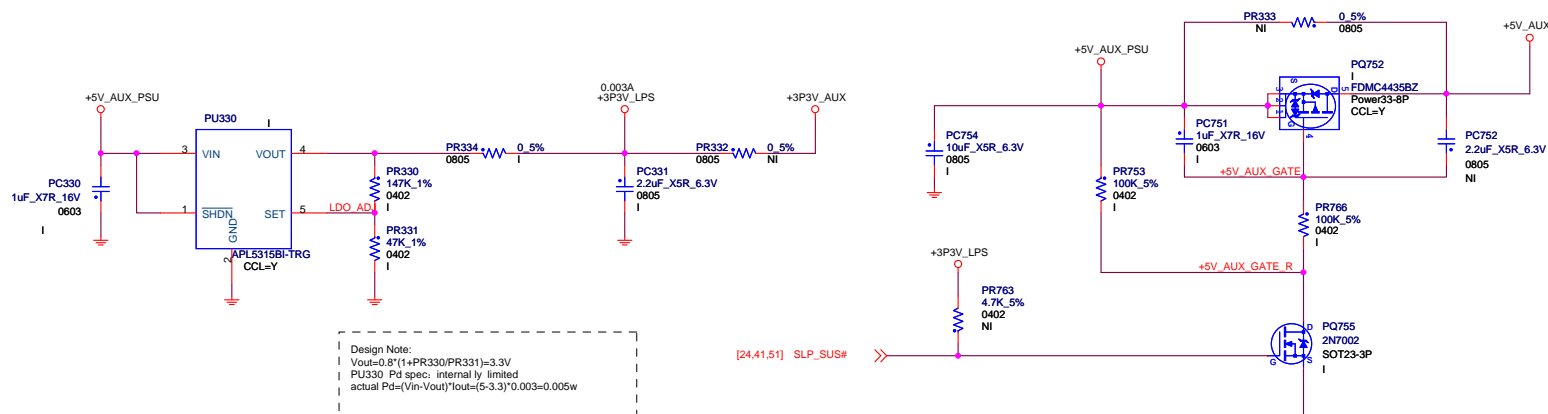












www.aitech1.ru

PCH GPIO Information

Name	Power Plane	Tolerance	Type	Default	Usage	Note
GPIO0 BMBUSY#	Core	3.3V	I/O	GPI	BMBUSY#	Pull up 10K to +3P3V.
GPIO1 TACH1	Core	3.3V	I/O	GPI	Non-Using	Pull up 10K to +3P3V.
GPIO2 PIRQ#	Core	5V	I/O	GPI	P_INT#	Pull up 8.2K to +3P3V.
GPIO3 PIRQF#	Core	5V	I/O	GPI	P_INT#	Pull up 8.2K to +3P3V.
GPIO4 PIRQ#	Core	5V	I/O	GPI	P_INT#	Pull up 8.2K to +3P3V.
GPIO5 PIRQH#	Core	5V	I/O	GPI	P_INT#	Pull up 8.2K to +3P3V.
GPIO6 TACH2	Core	3.3V	I/O	GPI	LPC_SMI#	Pull up 8.2K to +3P3V.
GPIO7 TACH3	Core	3.3V	I/O	GPI	BRD_ID3	Pull up 10K to +3P3V.
GPIO8	Suspend	3.3V	I/O	GPO	Non-Using	Pull down 1K to GND.(Reserved)
GPIO9 OC#	Suspend	3.3V	I/O	Native	USB_OC2_BACK#_LAN	Connect to USB OC circuit Note11
GPIO10 OC#	Suspend	3.3V	I/O	Native	USB_OC0_BACK#_1	Connect to USB OC circuit Note11
GPIO11 SMBALERT#	Suspend	3.3V	I/O	Native	SIO_PME#	Pull up 10K to +3P3V_AUX Note11
GPIO12 LAN_PHY_PWR_CTRL	Suspend	3.3V	I/O	Native	LAN_DISABLE#	Pull up 10K to +3.3V_AUX Option pull down 10K to GND Note8
GPIO13	Suspend	3.3V	I/O	GPI	Non-Using	Pull up 10K to +3P3V_AUX Note4
GPIO14 OC#	Suspend	3.3V	I/O	Native	USB_OC1_BACK#_2	Connect to USB OC circuit
GPIO15	Suspend	3.3V	I/O	GPO	PCH_OBSFN_C0(PROTO)	Pull up 1K to +3P3V_AUX
GPIO16 SATA0P	Core	3.3V	I/O	GPI	TCM_DIS#	Pull up 10K to +3P3V.
GPIO17 TACH0	Core	3.3V	I/O	GPI	Non-Using	Pull up 10K to +3P3V
GPIO19 SATA1GP	Core	3.3V	I/O	GPI	PCH_GP19_R	Pull up 10K to +3P3V.
GPIO20 PCIECLKRQ2#	Core	3.3V	I/O	Native	Non-Using	Pull up 10K to +3P3V
GPIO21 SATA0GP	Core	3.3V	I/O	GPI	F_AUDIO_DET#(Reserved)	Reserve 0 ohm to F_AUDIO_DET# Pull up 10K to +3P3V(If use this GPIO)
GPIO22 SCLCK	Core	3.3V	I/O	GPI	CLR_CMOS (Slotware)	Pull up 10K to +3P3V (For E2 Jumper)
GPIO23 LDRQ1#	Core	3.3V	I/O	Native	Non-Using	NONE(Test Point)
GPIO24 MEM_LED	Suspend	3.3V	I/O	GPO	SKTOCC#(Reserve)	Reserve 0 ohm to SKTOCC#
GPIO27	Deep Sleep	3.3V	I/O	GPI	Non-Using	Pull up 10K to +3P3V_LPS Option pull down 10K to GND
GPIO28	Suspend	3.3V	I/O	GPO	Non-Using	Pull down 1K to GND (Reversed)
GPIO29 SLP_LAN#	Suspend	3.3V	I/O	GPI	SLP_LAN#	Pull up 10K to +3P3V_AUX(Reserved) Note 10
GPIO30 SUSWARN#	Deep Sleep	3.3V	I/O	Native	SUS_WARN#	Pull up 10K to +3P3V_AUX(Reserved) Pull down 1K to GND(Reserved)
GPIO31	Deep Sleep	3.3V	I/O	GPI	Non-Using	Pull up 10K to +3P3V_LPS Note 6
GPIO32	Core	3.3V	I/O	GPO	TPM_DET#	Pull up 10K to +3P3V Note4
GPIO33	Core	3.3V	I/O	GPO	PRT_DET#	Pull up 10K to +3P3V Note4
GPIO34 STP_PC#	Core	3.3V	I/O	GPI	FRONT_USB_DET#_1	Pull up 10K to +3P3V

Name	Power Plane	Tolerance	Type	Default	Usage	Note
GPIO35	Core	3.3V	I/O	GPO	BRD_ID2	Pull down 10K to GND Option pull up 10K to +3P3V.
GPIO36 SATA2GP	Core	3.3V	I/O	GPI	Non-Using	N/A Option 10K Pull-up to +3P3V*
GPIO37 SATA3GP	Core	3.3V	I/O	GPI	GPIO37	Pull down 10K to GND Option pull up 10K to +3P3V.
GPIO38 SLOAD	Core	3.3V	I/O	GPI	CHASSIS_ID1	Pull up 10K to +3P3V
GPIO39 SDATAOUT0	Core	3.3V	I/O	GPI	BRD_ID1	Pull down 10K to GND Option pull up 10K to +3P3V.
GPIO40 OC1#	Suspend	3.3V	I/O	Native	USB_OC5_FRONT#1	Connect to USB OC circuit
GPIO41 OC2#	Suspend	3.3V	I/O	Native	USB_OC7_FRONT#3	Connect to USB OC circuit
GPIO42 OC3#	Suspend	3.3V	I/O	Native	Non-Using	Pull up 10K to +3P3V_AUX.
GPIO43 OC4#	Suspend	3.3V	I/O	Native	Non-Using	Pull up 10K to +3P3V_AUX.
GPIO44 PCIECLKRQ5#	Suspend	3.3V	I/O	Native	Non-Using	Pull up 10K to +3P3V_AUX
GPIO45 PCIECLKRQ6#	Suspend	3.3V	I/O	Native	Non-Using	Pull up 10K to +3P3V_AUX
GPIO46 PCIECLKRQ7#	Suspend	3.3V	I/O	Native	Non-Using	Pull up 10K to +3P3V_AUX
GPIO48 SDATAOUT1	Core	3.3V	I/O	GPI	CHASSIS_ID2	Pull up 10K to +3P3V
GPIO49 SATA5GP TEMP_ALERT#	Core	3.3V	I/O	GPI	PS2_DET#	Pull up 10K to +3P3V
GPIO50 REQ1#	Core	5.0 V	I/O	Native	P_REQ1#	Pull up 8.2K to +3P3V. Note11
GPIO51 GNT1#	Core	3.3V	I/O	Native	P_GNT1#	None
GPIO52 REQ2#	Core	5.0V	I/O	Native	Non-Using	Pull up 8.2K to +3P3V.
GPIO53 GNT2#	Core	3.3V	I/O	Native	Non-Using	Reserve 4.7K pull down to GND
GPIO54 REQ3#	Core	5.0 V	I/O	Native	Non-Using	Pull up 8.2K to +3P3V.
GPIO55 GNT3#	Core	3.3V	I/O	Native	Non-Using	Reserve 4.7K pull down to GND
GPIO57	Suspend	3.3V	I/O	GPI	Non-Using	Pull down 10K to GND Option pull up 10K to +3.3V_AUX
GPIO58 SML1CLK	Suspend	3.3V	I/O	Native	SML1CLK	Pull up 10K to +3P3V_AUX
GPIO59 OC0#	Suspend	3.3V	I/O	Native	USB_OC6_FRONT#2	Connect to USB OC circuit
GPIO60 SML0ALERT#	Suspend	3.3V	I/O	Native	Non-Using	Pull high 10K to +3P3V_AUX
GPIO61 SUS_STAT#	Suspend	3.3V	I/O	Native	TPM_LPD_PD#	Reserved 0 ohm resistor
GPIO62 SUSCLK	Suspend	3.3V	I/O	Native	Non-Using	Pull down 30 ohm to GND(Reserved)
GPIO63 SLP_S#	Suspend	3.3V	I/O	Native	SLP_S#	None
GPIO64 CLKOUTFLEX0	Core	3.3V	I/O	Native	Non-Using	NONE(Test Point)
GPIO65 CLKOUTFLEX1	Core	3.3V	I/O	Native	CK_P_14M_SIO	None
GPIO66 CLKOUTFLEX2	Core	3.3V	I/O	Native	CK_P_33M_TCM	None
GPIO67 CLKOUTFLEX3	Core	3.3V	I/O	Native	Non-Using	NONE(Test Point)
GPIO68 TACH4	Core	3.3V	I/O	GPI	FRONT_USB_DET#_2	Pull up 10K to +3P3V

Name	Power Plane	Tolerance	Type	Default	Usage	Note
GPIO69 TACH5	Core	3.3V	I/O	GPI	COMM_B_DETECT#	Pull up 10K to +3P3V
GPIO70 TACH6	Core	3.3V	I/O	Native	BOOT_BL_REC#	Pull up 8.2K to +3P3V Jumper pull low to GND(PROTO)
GPIO71 TACH7	Core	3.3V	I/O	Native	FRONT_USB_DET#_3	Pull up 10K to +3P3V
GPIO72	Suspend	3.3V	I/O	GPO	Non-Using	Pull up 10K to +3P3V_AUX Note4
GPIO74 PCHHOT# SML1ALERT#	Suspend	3.3V	I/O	Native	Non-Using	Pull up 2.2K to +3P3V_AUX Note11
GPIO75 SML1DATA	Suspend	3.3V	I/O	Native	SML1DATA	Pull up 2.2K to +3P3V_AUX Note11

Note4  
The functionality that is multiplexed with the GPIO may not be utilized in desktop configuration.

Note6  
In an Intel? ME disabled system, GPIO31 may be used as ACPRESENT from the EC.

Note8  
For GPIOs where GPIO vs. Native Mode is configured via SPI Soft Strap, the corresponding GPIO\_USE\_SEL bits for these GPIOs have no effect. The GPIO\_USE\_SEL bits for these GPIOs may change to reflect the Soft-Strap configuration even though GPIO Lockdown Enable (GLE) bit is set.

Note10.  
Once Soft-strap is set to GPIO mode, this pin will default to GP Input. When Soft-strap is SLP\_LAN# usage and if Host BIOS does not configure as GP Output for SLP\_LAN# control, SLP\_LAN# behavior will be based on the setting of the RTC backed SLP\_LAN# Default Bit (D31:F0:A4h:Bit 8).

Note11.  
When the multiplexed GPIO is used as GPIO functionality, care should be taken to ensure the signal is stable in its inactive state of the native functionality, immediately after reset until it is initialized to GPIO functionality

# SIO W83667 GPIO Information

Name	Power Plane	Tolerance	Type	Default	Usage	Note
GPIO10 VID0	Core	3.3V	I/O12t INg	VID0	Non-using	Pull down 0ohm to GND.
GPIO11 VID1	Core	3.3V	I/O12t INg	VID1	Non-using	Pull down 0ohm to GND.
GPIO12 VID2	Core	3.3V	I/O12t INg	VID2	Non-using	Pull down 0ohm to GND.
GPIO13 VID3	Core	3.3V	I/O12t INg	VID3	Non-using	Pull down 0ohm to GND.
GPIO14 VID4	Core	3.3V	I/O12t INg	VID4	Non-using	Pull down 0ohm to GND.
GPIO15 VID5	Core	3.3V	I/O12t INg	VID5	Non-using	Pull down 0ohm to GND.
GPIO16 VID6	Core	3.3V	I/O12t INg	VID6	Non-using	Pull down 0ohm to GND.
GPIO17 VID7	Core	3.3V	I/O12t INg	VID7	Non-using	Pull down 0ohm to GND.
GPIO20 KDAT	Suspend	3.3V	I/O12ts I/O16ts	KDAT	KBDDATA	Pull up 4.7K to +5V_DUAL_USB_B
GPIO21 KCLK	Suspend	3.3V	I/O12ts I/O16ts	KCLK	KBCLK	Pull up 4.7K to +5V_DUAL_USB_B
GPIO22 MDAT	Suspend	3.3V	I/O12ts I/O16ts	MDAT	MSDATA	Pull up 4.7K to +5V_DUAL_USB_B
GPIO23 MCLK	Suspend	3.3V	I/O12ts I/O16ts	MCLK	MSCLK	Pull up 4.7K to +5V_DUAL_USB_B
GPIO24 SLCT	Suspend	3.3V	I/O12ts INts	GPI	H_SLC	Pull up 2K to +5V_LPT2
GPIO25 AUXFANIN1	Suspend	3.3V	I/O12t I/O12t	AUXFANIN1	Non-Using	Pull down 1K to GND.
GPIO26 AUXFANIN2 SCE#	Suspend	3.3V	I/O12t I/O12t O12	AUXFANIN2	Non-Using	None
GPIO27 SCK	Suspend	3.3V	I/O12t O12	GPI	Non-Using	Pull up 4.7K to +3P3V_AUX
GPIO30 SUSC#	Suspend	3.3V	I/O12t INt	SUSC#	SLP_S4#	None
GPIO31 RESETCON#	Suspend	3.3V	I/O8t INt	RESETCON#	RESETCON#	Pull up 4.7K to +3P3V
GPIO32 PWROK0	Suspend	3.3V	I/O12t O012	PWROK0	PWROK0_140MS	Pull up 1K to +3P3V.
GPIO33 3VSB5W#	Suspend	3.3V	I/O12t O12	3VSB5W#	3VSB5W#	Pull up 10K to +3P3V_AUX
GPIO34 ATXPGD	Suspend	3.3V	I/O12t INt	ATXPGD	PWROK_PS	Pull up 4.7K to +5V
GPIO35 RSTOUT0#	Suspend	3.3V	I/O24t O024	RSTOUT0#	LATCHED_BKFD_CUT	Pull up 4.7K to +3P3V_AUX(Reserve)
GPIO36 RSTOUT1#	Suspend	3.3V	I/O24t O24	RSTOUT1#	Non-Using	Pull up 4.7K to +3P3V
GPIO37 SDA IRTX	Suspend	3.3V	I/O12ts I/O12ts O12	GPI	SML1DATA	Pull up 2.2K to +3P3V_AUX
GPIO40 RIB#	Suspend	3.3V	I/O12t INt	GPI	ARI2#	None
GPIO41 DCDB#	Suspend	3.3V	I/O12t INt	GPI	DCD2#	None
GPIO42 SOUTB	Suspend	3.3V	I/O12t O8	GPI	TXD2	None
GPIO43 SNB	Suspend	3.3V	I/O12t INt	GPI	RXD2	None
GPIO44 DTRB#	Suspend	3.3V	I/O12t O8	GPI	DTR2#	None
GPIO45 RTS#	Suspend	3.3V	I/O12t O8	GPI	RTS2#	None
GPIO46 DSR#	Suspend	3.3V	I/O12t INt	GPI	DSR2#	None
GPIO47 CTS#	Suspend	3.3V	I/O12t INt	GPI	CTS2#	None

Name	Power Plane	Tolerance	Type	Default	Usage	Note
GPIO50 SCL IRRX	Suspend	3.3V	I/O12t INts	GPI	SML1CLK	Pull up 2.2K to +3P3V_AUX
GPIO51 SUBS#	Suspend	3.3V	I/O12t INt	SUBS#	SLP_S3#	None
GPIO52 PSCH#	Suspend	3.3V	I/O12t O012	PSCH#	PSCH#_SIO	Pull up 1K to +5V_AUX(Reserved)
GPIO53 SUSLED	Suspend	3.3V	O8 O8	GPO	TEST2_EN	Pull down 47K to GND Option pull up 1K to +3P3V_AUX
GPIO54 PSIN#	Suspend	3.3V	I/O8t INt	PSIN#	PWRBTN#_SIO	Pull up 4.7K to +3P3V_AUX
GPIO55 PSOUT#	Suspend	3.3V	I/O12t O012	PSOUT#	PWRBTN_OUT#_SIO	Pull up 4.7K to +3P3V_AUX(Reserved)
GPIO56 SKTOCC	Suspend	3.3V	I/O12t INt	SKTOCC	SKTOCC#_S	Pull down 1K to GND Option pull up 1M to +3V_BATT
GPIO57 RSMRST#	Suspend	3.3V	I/O12t O012	DCDA#	SIO_RSMRST#	Pull up 1K to +3P3V_AUX Pull down 200K to GND
GPIO60 RI#	Core	3.3V	I/O12t INt	RSMRST#	ARI#	None
GPIO61 DCDA#	Core	3.3V	I/O12t INt	DCDA#	DCD1#	None
GPIO62 SOUTA FANSET	Core	3.3V	I/O12t O8 INcd	SOUTA	TXD1 LPT_PORT80W(Strap)	Pull up 1K to +3P3V Option pull down 1K to GND
GPIO63 SINA	Core	3.3V	I/O12t INt	SINA DTRA#	RXD1	None
GPIO64 PENROM DTRA#	Core	3.3V	I/O12ts INcd O8	DTRA#	DTR1# VID_EN(Strap)	Pull down 1K to GND Option pull up 1K to +3P3V
GPIO65 HEFRAS RTSA#	Core	3.3V	I/O12ts INcd O8	RTSA#	RTS1# 2E#_4E_SEL(Strap)	Pull down 1K to GND Option pull up 1K to +3P3V
GPIO66 DSRA#	Core	3.3V	I/O12t INt	DSRA#	DSR1#	None
GPIO67 CTS1#	Core	3.3V	I/O12t INt	CTS1#	CTS1#	None
GPIO70 VID00	Suspend	3.3V	I/O12t O012	VID00	Non-Using	Pull up 4.7K to +3P3V_AUX(Reserved)
GPIO71 VID01	Suspend	3.3V	I/O12t O012	VID01	Non-Using	Pull up 4.7K to +3P3V_AUX(Reserved)
GPIO72 VID02	Suspend	3.3V	I/O12t O012	VID02	Non-Using	Pull up 4.7K to +3P3V_AUX(Reserved)
GPIO73 VID03	Suspend	3.3V	I/O12t O012	VID03	Non-Using	Pull up 4.7K to +3P3V_AUX(Reserved)
GPIO74 VID04	Suspend	3.3V	I/O12t O012	VID04	DSW_EN(Strap)	Pull down 1K to GND Option pull up 8.2K to +3P3V_AUX
GPIO75 VID05	Suspend	3.3V	I/O12t O012	VID05	Non-Using	Pull down 1K to GND(Reserved)
GPIO76 VID06	Suspend	3.3V	I/O12t O012	VID06	Non-Using	Pull up 4.7K to +3P3V_AUX(Reserved)
GPIO77 VID07	Suspend	3.3V	I/O12t O012	VID07	Non-Using	Pull down 1K to GND(Reserved)
GPIO80 STB#	Suspend	3.3V	I/O12t O012	GPI	H_STB#	Pull up 2K to +5V_LPT2.
GPIO81 PECL_REG# AFD#	Suspend	3.3V	I/O12ts O012 O012	GPI	H_AFD#	Pull up 2K to +5V_LPT2
GPIO82 VID_RST# ERR#	Suspend	3.3V	I/O12ts INts	GPI	H_ERR#	Pull up 2K to +5V_LPT2
GPIO83 PLED INT#	Suspend	3.3V	I/O12ts O012 O012	PLED	H_PRNINT#	Pull up 2K to +5V_LPT2
GPIO84 BEEP SLIN#	Suspend	3.3V	I/O12t O012 O012	BEEP	H_SLIN#	Pull up 2K to +5V_LPT2
GPIO85 ACK#	Suspend	3.3V	I/O12t INts	GPI	H_ACK#	Pull up 2K to +5V_LPT2
GPIO86 BUSY	Suspend	3.3V	I/O12t INts	GPI	H_BUSY	Pull up 2K to +5V_LPT2
GPIO87 PE	Suspend	3.3V	I/O12t INts	GPI	H_PE	Pull up 2K to +5V_LPT2

Name	Power Plane	Tolerance	Type	Default	Usage	Note
GPIO80 PD0	Suspend	3.3V	I/O12t I/O12ts	GPI	H_PD0	Pull up 2K to +5V_LPT2
GPIO91 PD1	Suspend	3.3V	I/O12t I/O12ts	GPI	H_PD1	Pull up 2K to +5V_LPT2
GPIO92 PD2	Suspend	3.3V	I/O12t I/O12ts	GPI	H_PD2	Pull up 2K to +5V_LPT2
GPIO93 PD3 PWROK1	Suspend	3.3V	I/O12ts I/O12ts O012	PWROK1	H_PD3	Pull up 2K to +5V_LPT2
GPIO94 PD4	Suspend	3.3V	I/O12t I/O12ts	GPI	H_PD4	Pull up 2K to +5V_LPT2
GPIO95	Suspend	3.3V	I/O12t I/O12ts	GPI	H_PD5	Pull up 2K to +5V_LPT2
GPIO96 PD6	Suspend	3.3V	I/O12t I/O12ts	GPI	H_PD6	Pull up 2K to +5V_LPT2
GPIO97 PD7 PWROK2	Suspend	3.3V	I/O12t I/O12ts O012	PWROK2	H_PD7	Pull up 2K to +5V_LPT2

## I/O Type DESCRIPTION

ANUT - Analog output pin  
AIN - Analog input pin  
INcd - CMOS-level input pin with internal pull-down resistor  
INcs - CMOS-level input pin with internal pull-up resistor  
INcs - CMOS-level, Schmitt-trigger input pin  
INcsu - CMOS-level, Schmitt-trigger input pin with internal pull-up resistor  
INt - TTL-level input pin  
INg - TTL-level input pin with internal pull-down resistor  
INts - TTL-level, Schmitt-trigger input pin  
INtsu - 3.3V TTL-level Schmitt-trigger input pin  
INtsu - TTL-level input pin with internal pull-up resistor  
I/O8 - bi-directional pin with 8-mA source-sink capability  
I/O12 - TTL-level, bi-directional pin with 12-mA source-sink capability  
I/O12 - bi-directional pin with 12-mA source-sink capability  
I/O12t - TTL-level, bi-directional pin with 12-mA source-sink capability  
I/O12ts - Schmitt-trigger, bi-directional pin with 12-mA source-sink capability  
I/O12tp3 - 3.3V, TTL-level, bi-directional pin with 12-mA source-sink capability  
I/O08t - TTL-level, bi-directional pin. Open-drain output with 8-mA sink capability  
I/O012t - bi-directional pin. Open-drain output with 12-mA sink capability  
I/O012ts - CMOS-level, bi-directional, Schmitt-trigger pin. Open-drain output with 12-mA sink capability  
I/O012tp3 - 3.3V, TTL-level, bi-directional pin. Open-drain output with 12-mA sink capability  
I/O016t - TTL-level, bi-directional pin. Open-drain output with 16-mA sink capability  
I/O016ts - Schmitt-trigger, bi-directional pin. Open-drain output with 16-mA sink capability  
I/O016tsu - CMOS-level, Schmitt-trigger, bi-directional pin. Open-drain output with 16-mA sink capability  
I/O024t - TTL-level, bi-directional pin. Open-drain output with 24-mA sink capability  
I/O2p3 - 3.3V output pin with 12-mA source-sink capability  
I/O2p3 - 3.3V, TTL-level output pin with 12-mA source-sink capability  
I/O8 - TTL-level input pin with 8-mA source-sink capability  
I/O8 - TTL-level output pin with 8-mA source-sink capability  
O24 - TTL-level output pin with 24-mA source-sink capability  
O08 - Open-drain output pin with 8-mA sink capability  
O012 - Open-drain output pin with 12-mA sink capability  
O024 - Open-drain output pin with 24-mA sink capability  
I/v - Input pin with source capability of 6 mA and sink capability of 1 mA  
I/v0 - bi-direction pin with source capability of 6 mA and sink capability of 1 mA

# Lan WG82579LM GPIO Information

Name	Power Plane	Tolerance	Type	Default	Usage	Note
GPIO0	Lan VDD	3.3V	I/O		Non-Using	Pull up 4.7K to +3.3V_LAN
GPIO1	Lan VDD	3.3V	I/O		Non-Using	Pull up 4.7K to +3.3V_LAN

# Audio Codec GPIO Information

Name	Power Plane	Tolerance	Type	Default	Usage	Note
GPIO0	Audio DVDD	3.3V	I/O		AUD_GPIO0	Pull up 10K to +3P3V
GPIO1	Audio DVDD	3.3V	I/O		Non-Using	None

PCH Strapping Pins


Signal	Usage	When Sampled	Pull high Pull low	Comment															
SPKR	No Reboot	Rising edge of PWROK	Pull down	The signal has a weak internal pull-down. Note: The internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Cougar Point will disable the TCO Timer system reboot feature). The status of this strap is readable via the NO REBOOT bit (Chipset Config Registers: Offset 3410h:Bit 5).															
INIT3_V#	Reserved	Rising edge of PWROK	Pull up	This signal has a weak internal pull-up. Note: The internal pull-up is disabled after PLTRST# deasserts.NOTE: This signal should not be pulled low															
QNT7# / GPIO55	Top-Block Swap Override	Rising edge of PWROK	Pull up	The signal has a weak internal pull-up. Note: The internal pull-up is disabled after PLTRST#deasserts. If the signal is sampled low, thisindicates that the system is strapped to the "topblock swap" mode (Cougar Point inverts A16 for all cycles targeting BIOS space).The status of this strap is readable via the Top Swap bit (Chipset Config Registers: Offset 3414h:Bit 0). Note that software will not be able to clear the Top-Swap bit until the system is rebooted without QNT7# being pulled down.															
INTVSMEN	Integrated 1.05 V VRM Enable / Disable	Always	Pull up	Integrated 1.05 V VRMs is enabled when high NOTE: This signal should always be pulled high															
QNT1#/ GPIO51/ BSEL	Boot BIOS Strap bit 1 BSEL	Rising edge of PWROK	Pull up	This Signal has a weak internal pull-up. Note: The internal pull-up is disabled after PLTRST# deasserts.This field determines the destination of accesses to the BIOS memory range. Also controllable via Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:Bit11). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. <table><tr><td>Bit11</td><td>Bit 10</td><td>Boot BIOS Destination</td></tr><tr><td>0</td><td>1</td><td>Reserved</td></tr><tr><td>1</td><td>0</td><td>PCI</td></tr><tr><td>1</td><td>1</td><td>SPI</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></table> NOTE: If option 00 LPC is selected BIOS may still be placed on LPC, but all platforms with Cougar Point require SPI flash connected directly to the Cougar Point's SPI bus with a valid descriptor in order to boot.  NOTE: Booting to PCI is intended for debug/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel® ME or Integrated GBE LAN. NOTE: PCI Boot BIOS destination is not supported on Mobile	Bit11	Bit 10	Boot BIOS Destination	0	1	Reserved	1	0	PCI	1	1	SPI	0	0	LPC
Bit11	Bit 10	Boot BIOS Destination																	
0	1	Reserved																	
1	0	PCI																	
1	1	SPI																	
0	0	LPC																	
SATA1GP/ GPIO19	Boot BIOS Strap bit 0 BBS0	Rising edge of PWROK	Pull up	This Signal has a weak internal pull-up. Note: The internal pull-up is disabled after PLTRST# deasserts.This field determines the destination of accesses to the BIOS memory range. Also controllable via Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:Bit10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. <table><tr><td>Bit11</td><td>Bit 10</td><td>Boot BIOS Destination</td></tr><tr><td>0</td><td>1</td><td>Reserved</td></tr><tr><td>1</td><td>0</td><td>PCI</td></tr><tr><td>1</td><td>1</td><td>SPI</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></table> NOTE: If option 00 LPC is selected BIOS may still be placed on LPC, but all platforms with Cougar Point require SPI flash connected directly to the Cougar Point's SPI bus with a valid descriptor in order to boot.  NOTE: Booting to PCI is intended for debug/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel® ME or Integrated GBE LAN. NOTE: PCI Boot BIOS destination is not supported on Mobile	Bit11	Bit 10	Boot BIOS Destination	0	1	Reserved	1	0	PCI	1	1	SPI	0	0	LPC
Bit11	Bit 10	Boot BIOS Destination																	
0	1	Reserved																	
1	0	PCI																	
1	1	SPI																	
0	0	LPC																	
QNT2#/ GPIO53	ESI Strap (Server Only)	Rising edge of PWROK	Pull up	This Signal has a weak internal pull-up. NOTE: The internal pull-up is disabled afterPLTRST# deasserts.Tying this strap low configures DMI for ESIcompatible operation. NOTE: ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.															
HDA_SDO	Flash Descriptor Security Override/ ME Debug Mode	Rising edge of RSMRST#	Pull down EI jump to Pull up	Signal has a weak internal pull-down. If strap is sampled low, the security measures defined in the Flash Descriptor will be in effect (default). If sampled high, the Flash Descriptor Security will be overridden. This strap should only be asserted high via external pull-up in manufacturing/debug environments ONLY. NOTE: The weak internal pull-down is disabled after PLTRST# deasserts. NOTE: Asserting the HDA_SDO high on the rising edge of RSMRST# will also halt Intel® Management Engine after chipset bringup and disable runtime Intel ME features. This is a debug mode and must not be asserted aftermanufacturing/debug.															
DP_TV5	For future processor compatibility	Rising edge of PWROK	Pull up	Pull-Up: For future processor compatibility This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.															
GPIO28	On-Die PLL Voltage Regulator	Rising edge of RSMRST# pin	Pull up	This signal has a weak internal pull-up. NOTE: The internal pull-up is disabled after RSMRST# deasserts. The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled.															
HDA_SYNC	On-Die PLL Voltage Regulator Voltage Select	Rising edge of RSMRST# pin	Pull down	This signal has a weak internal pull-down. On Die PLL VR is supplied by 1.5 V when sampled high, 1.8 V when sampled low.															
GPIO15	TLS Confidentiality	Rising edge of RSMRST# pin	Pull up	Low = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel ME Crypto TLS cipher suite with confidentiality This signal has a weak internal pull-down. NOTE: The weak internal pull-down is disabled after RSMRST# deasserts. NOTE: A strong pull-up may be needed for GPIO functionality															
SDVO_CTRLDA TA	Port B Detected	Rising edge of PWROK	Pull down	When '1'- Port B is detected: When '0'- Port B is not detected This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.															
DDPC_CTRLDA TA	Port C Detected	Rising edge of PWROK	Pull up	When '1'- Port C is detected: When '0'- Port C is not detected This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.															
DDPD_CTRLDA TA	Port D Detected	Rising edge of PWROK	Pull down	When '1'- Port D is detected: When '0'- Port D is not detected This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.															

Signal	Usage	When Sampled	Pull high Pull low	Comment
DSWVRMEN	Deep S4/S5 Well On-Die Voltage Regulator Enable	Always	Pull up	If strap is sampled high, the Integrated Deep S4/S5 Well (DSW) On-Die VR mode is enabled.
SATA2GP/ GPIO36	Reserved	Rising edge of PWROK	N/A	This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled high when strap is sampled.
SATA3GP/ GPIO37	Reserved	Rising edge of PWROK	N/A	This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled high when strap is sampled.

SIO NCT6681D Strapping Pins

Signal	Usage	When Sampled	Pull High/Low	Description
Pin33 - Strap0 - SCKI#	SCKI# (SPI Interface)	TBD	Pull down 1K ± Rxx	Pull High: - XOR Tree Mode Enable.  Pull Down: - SPI Interface Enable
Pin34 - Strap1 - SCKI	SCKI (SPI Interface)	TBD	Pull down 1K ± Rxx	Pull High: - PS2 Port Tri-State Enable and KBC Disable.  Pull Down: - SPI Interface Enable

www.aitech1.ru

**Foxconn CMMSSG**  
Foxconn Wuhan  
China

Hon Hai Precision Industry Co. Ltd.  
  
Phone: 755-28128888 Ext:22280  
Fax: +86-755-2812-8888

Title**PCH/SIO Strapping Pins**

Size C Document Number**IS6XM uATX**Rev**X7**

Page Modified: Wednesday, December 08, 2010 16:17:01 (UTC+0800) Sheet 54 of 55

Change List From Pre-SDV to SDV BOM Ver:0.1 Schematic

- 1.Non-Install CK505 Cicuit component related.  
- Non-Install almost component in Page 9  
- Keep SATA/96M/DMI/14M clock pull-low resistor (R730,R731,R632,R733,R734,R735,R736) from PCH guideline.
- 2.Change Mono-Out BOM parameter from Proto to I meet Customer spec  
- Insaatl Mono-Out block component in page33
- 3.Change PCH Heatsink to Meet Customer Spec  
- Follow Intel Reference Design. (PM:VSB10602A-01)
- 4.The SuperIO integrate "SUS\_PWR\_ACK#\" for PCH  
- Change BOM parameter from I to Proto that Using SuperIO integrate circuit.  
- NI R1416,R1419 to isolate SuperIO.  
- Connect PCH's "SUS\_WARN#\" to SuperIO Pin.82  
- Add "+5V\_DUAL\_USB\_B\" monitor circuit (R35,R36) connect to SuperIO's VIN1 Pin.100
- 5.The SuperIO integrate SM Bus switch.  
- Delete discrete SM Bus switch circuit in page38.  
- The SuperIO Pin74,75 for MainPower rail  
- The SuperIO Pin73,72 for AuxPower rail  
- Add serial resistor R357,R361(33ohm) avoid "Y\" topology layout.
- 6.The SuperIO integrate "PWRGD\_30MS\" for power rail control  
- Delete discrete 30ms delay circuit in page30.  
- Original control power rail by "PWRGD\_30MS\" change to SuperIO's PWROK1 Pin122.
- 7.Fixed SuperIO Leakage issue in S5  
- Add R311 Pull up to 3P3V\_AUX at XIN PIN
- 8.Fix LP05V\_ME to PCH\_MEPWROK sequence fail from So to S5  
-Change R119 from 200K to 4.7K
- 9.Fix PLT\_RST# at SIO point overshoot issue  
-Change R391 from 0ohm to 33ohm
- 10.Fix PCH\_DPPWROK delay time can not meet the sequence with +3P3V\_LPS  
-R1412 from 47K to 56K increase the delay time
- 11.Reserve/Add SuperIO's SPI interface pull-up resistor  
- Reserve R1(8.2K) pull-up to 3.3VAUX at "S\_SPI\_CS#\" Pin  
- Add R2(8.2K) pull-up to 3.3VAUX at "S\_SPI\_M#\"
- 12.Fix PWR\_FAN can't control issue  
- Connect PWR\_FAN signal "PWR\_FAN\_PWM/PWR\_FAN\_TACH\"to SIO PIN88/94  
- Del R240 pull down resistance to SIO PIN94
- 13.Fix LED control pin OD need pull up issue  
- Install R3256,R3257
- 14.Fixed VGA ESD Issue that add protect diode in each VGA pin  
- D6,D7,D8,D9 for "H/V Sync\" and "DDC\_Data/CLK\" close connector  
- D2,D4,D5 for R,G,B close connector after filter.
- 15.Fix DDR3\_DRAMRST# no-monotonic issue that add discrete buffer  
- Non-Install R440, R737 isolate MCP and DIMM slot  
- Add discrete Buffer circuit in pagell
- 16.Fix SLP\_S3# No-monotonic issue  
- Add R228 avoid the "Y\" topology layout.
- 17.Fix PS0N# sequence Issue that change control from "SLP\_SUS#\" to "SIO\_RSMRST#\"  
- Change "SLP\_SUS#\" to "RSMRST#\" For R3302.1 in page41
- 18.Avoid SYS\_PWRGD to SUS\_STATE# Sequence less than 1ms spec.  
- Change PC381 From I to NI, reduce SYS\_PWRGD slope rate
- 19.Improved ST L6738's CSN Noise add 100nF cap in CSN pin.  
- PC509 for "+LP05V\_ME\"  
- PC482 for "+LP5V\_DUAL\"  
- PC613 for "+VCCIO\"  
- PC543 for "+VCCSA\"
- 20.Improve VCCSA compensation  
- PR536 change 4.7K\_1# to 4.12K\_1#  
-PC537 change 2.2nF\_X7R\_50V to 330pF\_X7R\_50V  
-PC540 change 22nF\_X7R\_16V to 3.3nF\_X7R\_50V
- 21.Improve VCCIO transient  
- Add E-CAP PCB608 (820uF) for output.  
- Reserved PL606 colay with PL605  
- Add PCB14
- 22.Because of NTMFS4841NNT1G will EOL for VCORE /VCC\_AGX/VCC\_DDR  
- PQ211, PQ221, PQ231, PQ241, PQ270, PQ470 change from NTMFS4841NNT1G to NTMFS4921NT3G
- 23.Fix VCORE /VCC\_AGX input choke nosie issue  
- PL200 change to APL0806P7C-R90L

Change List From SDV BOM Ver:0.1 to Ver:0.2 Schematic

- 1.Correct BIOS Licence Label to AMI uEFI  
- change P/N 1332 to 1431
- 2.Change some P/N to standard P/N ..

Change List From SDV BOM Ver:0.2 to Ver:0.3 Schematic

- 1.Correct Manchester uATX BIO to "0 0 0\" follow customer require  
- Non-Install BRD\_BID3 Pull up resistance R441
- 2.Change Mono-Out BOM parameter from Proto to I meet Customer spec  
- Insaatl Mono-Out block component in page33
- 3.For good performance to vcore and AGX power  
-PQ215 , PQ216, PQ225, PQ226 , PQ235, PQ236, PQ245, PQ246, PQ275, PQ276 change from I to NI,  
-PQ217, PQ218, PQ227, PQ228, PQ237, PQ238, PQ247, PQ248, PQ277, PQ278 change from NI to BSC886N03LS G  
-PQ211,PQ221,PQ231,PQ241,PQ270,change NTMFS4921NT3G to BSC079N03LSC G
4. For good performance to +1P5V\_DUAL power  
-PQ470 change from I to NI, PQ471 change from NI to I
- 5.To fix +5V\_AUX\_F5U drop issue  
-PR766 change from 1K\_5# to 10K\_5#  
-PC754 change to I  
-PC751 change from 1uF\_X7R\_16V to 10uF\_X5R\_6.3V  
-PR314, PR315, PU302, PR313, PR302, PR303, PR304, PC302, PC301 change from I to NI,  
-PCE300 change to I with 470uF\_EC\_16V
6. For marking IC version of VCORE  
-FU100 change from NCP6151S52MNR2G to NCP6151S52MNR2G PC9
- 7.To meet vcore LL fail and AGX ripple fail issue  
-PR102 change from 7.15K\_1# to 7.5K\_1#  
-FR148 change from 9.09K\_1# to 8.2K\_1#
8. For NCP5901MNR2G version change to support BST diode integrated driver  
-PU210, PU220, PU230, PU240, FU270 change from NCP5901MNR2G to NCP5901BMVTBG  
-PD210, PD220, PD230, PD240, PD270 change from I to NI
9. To meet VCCIO ACLL spec  
-PR608 change from 4.7K\_1# to 4.99K\_1#  
-PC611 change from 2.2nF\_X7R\_50V to 10nF\_NPO\_50V  
-PC606 change from 22nF\_X7R\_16V to 10nF\_X7R\_16V  
-PR611 change from 10\_1# to 100\_1#  
-PR601 change from 47K\_1# to 35.7K\_1#  
-PC614 change from 1.5uF\_X7R\_50V to 470pF\_X7R\_50V  
-C561, C589 change from NI to I in P14
10. To improve snubber C value precision for vcore and +VCC\_AGX power  
-PC211, PC221, PC231, PC241, PC271 change from 4.7n F/+/-20% to 4.7n F/+/-10%
11. For good performance base on current layout to +VCC\_AGX power,  
-PC274 change from I to NI, PC276 change from NI to I
12. increare Q230 Vbe voltage for Q230 enter saturation states at low temperature safely  
-Change R304 from1.1K to 1.54K,Vbe(max)=1.06V


Change List From SDV BOM Ver:0.3 to Ver:0.4Schematic

- 1.Increare Q230 Vbe voltage for Q230 enter saturation states at low temperature safely  
-Change R304 from1.54K to 1.4K,Vbe(max)=0.9V
- 2.For VMD driver controller shortage  
- Change NCP5901BMVTBG to NT55901MNR2G
- 3.Fix Watch Ripple on Lenovo Special Monitor  
- Change +3P3V\_PCH\_DAC power source from +1.3V to liner power

Manchester ET to Pre-SDV Layout Change List

- 1.Correct Mechanical Issue from Lenovo  
- Change Mounting Hole from 4.4mm to 3.96+/-0.05mm  
- Move CI header to close SYS\_FAN.  
- Change J6(P52 Header) and PU20(4PIN Power) location follow lenovo recommend.  
- Change J74(THER\_ID) Location from Lenovo recommend.  
- Change I/O edge space to PCB edge meet 1.2mm spec  
- Move F\_USB1 & F\_USB2 together
- 2.Avoiding the crosstalk Issue.  
- Change H\_PWRGOOD net far away FLT\_RST# ,Avoiding the crosstalkrecommend.  
- Change I/O edge space to PCB edge meet 1.2mm spec  
- Move F\_USB1 & F\_USB2 together

www.aitech1.ru

		Hon Hai Precision Industry Co. Ltd.	
Foxconn CMMSG		Phone: 755-28128988 Ext:22260	
Foxconn WuHan		Fax: +86-755-2812-8988	
China			
Title			
Change List			
Size	Document Number	Rev	
Custom	IS6XM uATX	X7	
Page Modified: Wednesday, December 08, 2010		16:17:51 (UTC+8MT)	Sheet 65 of 65